Interfacial Studies in Organic Field-Effect Transistors

Zhang Jia

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ABSTRACT

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Organic field-effect transistors (OFETs) are potential components for large-area electronics because of their attractive advantages: light weight, cost-effective and large-area processability, flexibility and resonable performance potential. However, the commercialization of OFETs faces several technical obstacles. Low mobility of organic semiconductors limits the current-carrying capacity; high operation voltage restricts their use in many applications; easy degradation in air and instability under electrical stress usually make the lifetime too short to be useful; and contact resistance and contact matching also limit the charge injection to the semiconductor.

Many of the above problems relate to interfaces in OFETs. There are two important interfaces in OFETs. The interface between organic semiconductor and the dielectric layer is of crucial importance since it is the location where charge transport in the channel occurs. The other important interface in OFETs is between the semiconductor and the contacts, where the charge injection and removal happen during device operation. Surface treatment of the contacts for bottom-contact devices is usually necessary to achieve both a good semiconductor microstructure and excellent contact performance.

Great effort has been applied to improving device performance, primarily by focusing on enhancing device mobility to increase current capacity and improving subthreshold behavior to reduce the operation voltage. One approach to improving both figures of merit is to use a high-capacitance gate dielectric, which reduces the operating voltage and increases the mobile charge carrier density for a given gate voltage. Operating at a higher channel charge density improves the effective mobility in OFETs. I first demonstrate the use of nanoscale high-κ materials based on barium titanate (BT) which are normally ferroelectric as gate

dielectrics where their high dielectric constant is desirable but ferroelectric hysteresis is not.

Self-assembled monolayer (SAM) treatment of the dielectric has been used to improve the morphology of subsequent deposition of organic semiconductor. The dipoles within the SAM, however, dramatically change the electrical performance in terms of threshold voltage and mobility. This thesis reviews the SAM treatment and explains why there is a substantial change in threshold voltage. During the fabrication, reactive agents can also reside at the interface between the semiconductor and the dielectric layer. Their chemical and structural effects are minor but their effect on electrical performance can be significant. This problem is studied using spectral photocurrent and $1/f$ noise measurement by comparing OFETs whose polymer gate dielectric is exposed to UV ozone prior to semiconductor deposition with control OFETs whose semiconductor/dielectric interface is produced in a nearly oxygen-free environment. Both of the techniques have shown that the interfacial trapping sites created by oxygen treatment play an important role in electrical performance.

One approach developed to improve the performance of bottom contact source/drain electrodes is to treat the contacts with thiols before deposition of the semiconductor. Especially suggestive evidence shows that thiols that increase the effective work function of the contacts (*e.g.* fluorinated thiols) yield better device performance than work function decreasing thiols (*e.g.* alkane thiols). We compare two technologically relevant thiol treatments, an alkane thiol (1-hexadecanethiol), and a fluorinated thiol (pentafluorobenzenethiol), in pentacene organic field effect transistors. Using *in-situ* semiconductor deposition, X-ray photoemission, and X-ray absorption spectroscopy, we were able to directly observe the interaction between the semiconductor and the thiol-treated gold layers. Our spectroscopic analysis suggests that there is not a site-specific chemical reaction between the pentacene and the thiol molecules. A homogeneous standing-up pentacene orientation was observed in both treated substrates, consistent with the morphological improvement expected from thiol treatment in both samples. Our study shows that both the HOMO-Fermi level offset and C $1s$ binding energy are shifted in the two thiol systems, which can be explained by varied dipole direction within the two thiols, causing a change in surface potential. The additional improvement of the electrical performance in the pentafluorobenzenethiol case is originated by a reduced hole injection barrier that is also associated with

an increase of the density of states in the LUMO.

In OFETs, the accumulated charges are not evenly distributed along the channel especially when the OFETs are operated in the saturation region, where the drain side has much fewer accumulated charges than the source side due to the cancellation of effective gate voltage by the drain voltage. Thus the carriers should be less mobile on the drain side where the trap states are filled less adequately, and one should expect a varied mobility across the channel. For the same reason, the saturation current formula $I_{DS} = \frac{W}{2L}\mu C_i(V_{GS} - V_{th})^2$ for silicon MOSFETs is not suitable for OFETs, and the mobility calculation based on linear fitting of $\sqrt{I_{DS}}$ to V_{GS} is problematic. In the last part of this thesis, I have reviewed the curve fitting method and quasi-static capacitance-voltage (QSCV) method for deriving linear mobility in OFETs. Further, we have measured spatially resolved photocurrent in OFETs operated in the linear and saturation regions. Because the photogenerated charge is constant as a function of bias, spatially resolved photocurrent measurement locally measures the product of channel field and mobility. This product can be used to derive the local mobility across the channel. Our results directly show that in the saturation region, mobility decreases from source contact to drain contact due to the decreased density of carriers on the drain side.

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To my parents.

Chapter 1

Introduction

1.1 Background and motivation

Organic field effect transistors (OFETs) are potential components for large-area electronics because of their attractive advantages: low temperature and large-area processability, flexibility, and prospective performance potential. Their applications include flexible displays,[14] large area force sensing,[15] ultrasonic mapping,[16] and active matrix imaging.[17] [18]

The commercialization of OFETs, however, faces several technical obstacles. The low mobility of organic semiconductor limits the current-carrying capacity; the high operation voltage restrict their use in many applications; easy degradation in air and instability under stress usually make their lifetime too short to be useful; and contact resistance and contact matching also limit the charge injection to the semiconductor.

Many of above problems relate to interfaces in OFETs. There are two important interfaces in OFETs. The interface between organic semiconductor and the dielectric layer is of crucial importance since it is the location where charge transport in the channel occurs. The gate dielectric layer controls the charge density induced in the channel by the gate voltage. It is known [19] that most organic semiconductors [polycrystalline small molecule based semiconductors, e.g., pentacene, and polymer based semiconductors, e.g., poly 3-hexylthiophene (P3HT)] have bias-dependent mobilities where the mobility value depends on the channel charge density. A high-κ gate dielectric material, because of its high capac-

itance, can significantly boost the mobility of organic semiconductor even at low voltages. The selection of gate dielectric materials should also provide a favorable interface for the semiconductor to form appropriate microstructure necessary for reliable charge transport. Degradation of organic electronic devices happens when the organic semiconductors reacts with reactive agents such as oxygen and water, especially under intense illumination. In this kind of degradation, a chemical reaction directly affects or deteriorates the microstructure and electrical performance. During the fabrication, reactive agents can also reside at the interface between the semiconductor and the dielectric layer. Their chemical or structural effect is minor, but their effect on electrical performance can be significant. The other important interface in OFETs is between the semiconductor and the contacts, where the charge injection and removal happen during device operation. Surface treatment of the contacts for bottom-contact devices is usually necessary to achieve both a good semiconductor microstructure and excellent contact performance.

1.2 Objectives and approach

One approach that can both improve the mobility and reduce the operation voltage in OFETs is to use a high-κ gate dielectric. I demonstrate low-voltage OFETs on flexible substrates by incorporating self-assembled high-κ nanocrystals and high-κ polymers in the gate dielectric layer. In order to study the effects of reactive agents residing at the interface between the semiconductor and the dielectric, I apply spectral photocurrent and 1/f noise measurements in OFETs under different gate bias and illumination conditions. By using synchrotron X-ray photoemission and photoabsorption spectroscopies, I explain why thiols treatment can improve contact performance between the semiconductor and the contacts. It is worth noting that these studies and techniques can be applied directly to other organic and inorganic thin film devices, such as solar cells, light emitting diodes, and photodectors.

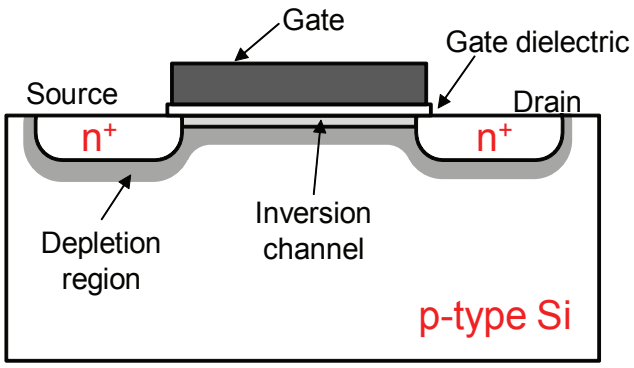

Figure 1.1: Basic elements of an n-channel p-substrate MOSFET.

1.3 Basic concepts in OFETs

1.3.1 How OFETs work

Before introducing OFETs operation, metal-oxide-semiconductor field-effect transistor (MOSFET) operation is reviewed. In an n-channel MOSFET (Fig. 1.1), for example, parts of a p-type silicon substrate are n^+ doped to form source and drain contacts. The thin region between the source and drain contacts is the channel. Above the channel are the gate dielectric and gate contact. Based on a rough simplification, with a negative gate bias, a layer of positive charges are accumulated at the interface. This is called the accumulation region and there is no current flowing because the source and drain are both n^+ doped and only conduct electrons. Within a slight positive voltage, all the carriers at the interface are depleted (depletion region) and still no current flows. With large enough positive gate voltage, an n-type inversion layer at the interface provides a conducting channel and a current is formed. So, in general, MOSFETs are operated in inversion mode.

OFETs or organic thin film transistors (OTFTs) operate in a drastically different - and simpler - manner. OFETs operate only in the accumulation region. In a top-contact structure scheme with a p-type semiconductor shown in Fig. 1.2, when a positive gate bias is applied, only negative charges are induced at the interface, and since pentacene conducts only holes (to be covered later), the device is off. Under negative gate bias, holes are attracted from the semiconductor to the interface, where a conducting channel is formed.

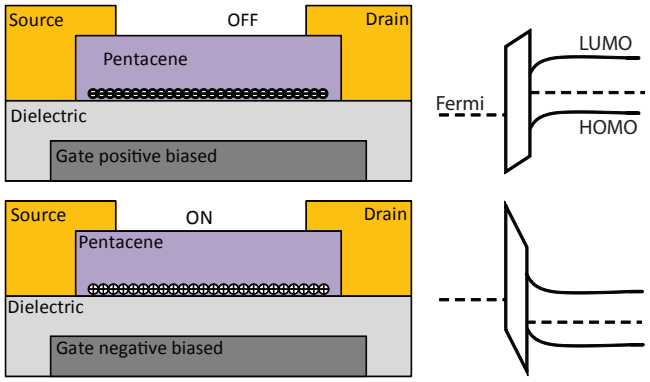

Figure 1.2: Schematics illustrating how an OFET works.

There is no inversion in OFETs; the low off current is only attributed to the low conductivity of the semiconductor material.

1.3.2 Organic semiconductor - pentacene

Pentacene is a p-type semiconductor: it transports holes because it is easier for a pentacene molecule to lose an electron than to accept an electron. Unlike the σ bond which is localized to two adjacent carbon atoms, the π electrons are shared and delocalized among a pentacene molecule, making losing such an electron is not energetically significant.

The conduction in pentacene is mainly limited by inter-molecule transitions. The band structure found in single crystal Si is replaced with molecular energy levels. There is also a molecular energy gap in pentacene between the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO), but this gap is not caused by interaction among the molecules but by the nature of molecular orbitals within a molecule. Calculations also predict that the mean free path would be smaller than the mean molecular distance in pentacene because of strong phonon and electron interaction.[20] This confirms that transport of carriers is through hopping of charges between localized states of individual molecules.

The exact transport mechanism in pentacene transistor is still in debate. A multiple trapping and release (MTR) model,[20] [21] used to describe amorphous Si TFTs, has been applied in OFETs [22] to understand the transport. A prominent similarity of amorphous

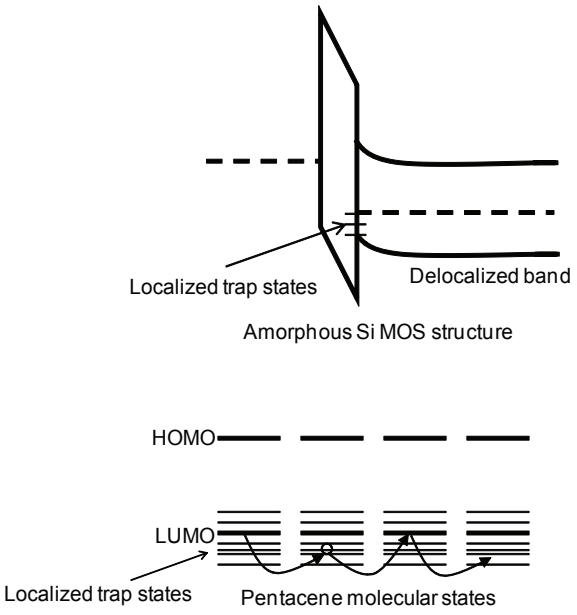

Figure 1.3: Multiple trapping and release (MTR) model for amorphous Si and pentacene

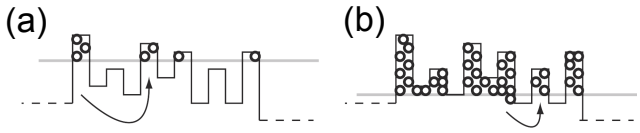

Figure 1.4: Schematics illustrating charge transport in pentacene from reference [1]. In (a), where the device is less accumulated, mobile carriers are activated from the deeper states and see a higher barrier to movement. In (b), as carriers fill the deeper trap states, more carriers are near the mobile carrier edge and are able to move with greater ease. The effective mobility is a function of the accumulated carrier density.

Si and pentacene is that the mobility is gate bias dependent. Amorphous Si also operates in the accumulation mode, where the applied gate voltage bends the valence and conduction bands and the Fermi level approaches the nearest delocalized band (valence band for p-type and conduction band for n-type). The carriers are excited thermally to this delocalized conduction band. There exists, near the delocalized band, a density of localized levels, which act as traps for carriers. At low gate bias, the accumulated charges fill these traps and their mobility is very low. As the gate bias increases, the localized traps are filled as the concentration of carriers in the delocalized band increases. As a result, the effective mobility increases.[20] [23] In pentacene, however, all the molecular states are localized and there is no delocalized band among molecules (Fig. 1.3). Electrically, the exact HOMO-LUMO positions within a molecule are not the determining factors for carrier conduction. A schematic depiction of carrier transport in shown in Fig. 1.4

Microstructure plays an important role in pentacene performance. Fig. 1.5 is a summary of the relation between pentacene structure and performance taken from [2]. Crystalline pentacene has a stacked structure with standing-up molecular orientation. There are two phases in pentacene crystalline structures: the single crystal phase with a 001 plane spacing of 14.5 Åand the thin film phase with a 001 plane spacing of 15.4 Å. When the deposition rate is too high and the substrate is kept at a very low temperature, the evaporated pentacene molecule does not have enough mobility at the substrate surface to form crystalline structure and the mobility is very low. The best performance structure is a single phase thin

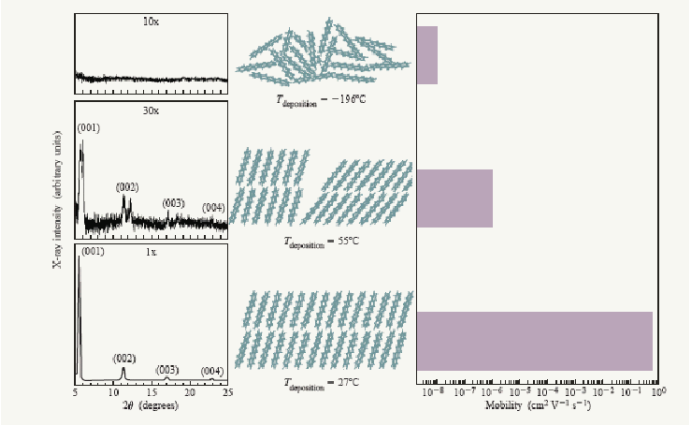

Figure 1.5: Deposition Temperature effect on the microstructure and mobility of pentacene from reference[2]

film structure or single crystalline structure. There is abundant literature [24] [25] studying the relation between processing parameters and the pentacene performance. It is worth mentioning that the specific conditions used by individual groups are not universal; the performance always depends on the characteristics of particular evaporation systems and setups. Grains and grain boundaries are important in polycrystalline Si devices because the grain boundaries are the limiting factors for transport. This is not the case for OFETs. As previously mentioned, the transport limitation is mainly inter-molecule transitions. Pentacene with small grains can have much better mobilities than that with large grains.[21] More discussion about pentacene morphology on different dielectric surfaces is continued in chapter 3.

1.3.3 Basic OFETs operation model and parameter extraction

Fig. 1.6 (a) shows a typical curve for I_{DS} vs. V_{DS} under different V_{GS} in an OFET device. Fig. 1.6 (b) shows the I_{DS} vs. V_{GS} in saturation operation regime under V_{DS}=-40 V. This particular device has an on-off ratio of approximately 10^5 and a subthreshold of 3 V/decade.

Despite the difference of conduction mechanism, the OFETs transport curves can be depicted by similar formula used in MOSFETs. Take a slice in the channel shown in Fig.

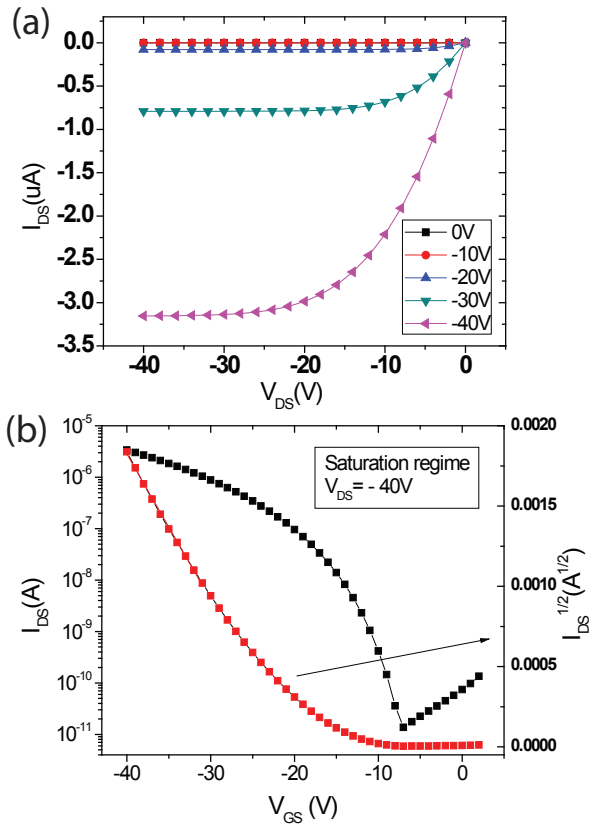

Figure 1.6: (a)Typical curve for I_{DS} vs. V_{DS} under different V_{GS} (b)I_{DS} vs. V_{GS} in saturation operation regime

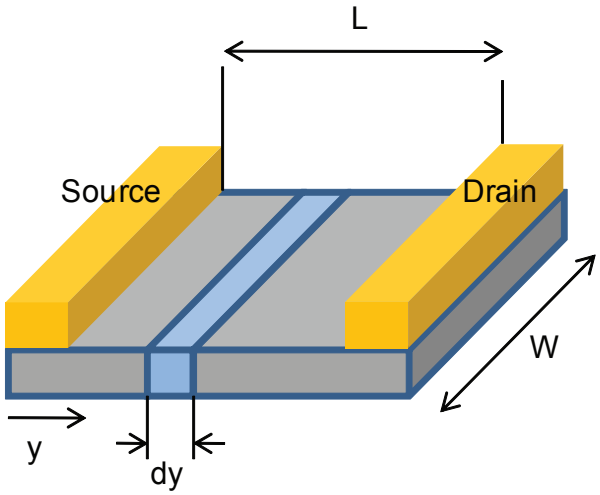

Figure 1.7: Derivation of drain current in OFET channel.

1.7. For any position y along the channel, the drain current

$$I_{DS}(y) = \frac{\Delta Q}{\Delta t} = \frac{Q \cdot dy \cdot W}{dt} \tag{1.1}$$

where W is the channel width, Q is the capacitive charge density and $Q = (V_{GS} - V_{th} - V_{ch})C_i$ (V_{GS} is the gate voltage, V_{th} is the threshold voltage, C_i is the dielectric capacitance per unit area, V_{ch} is the channel voltage and is a function of position y). Since charge velocity $v = dy/dt = \frac{dV_{ch}(y)}{dy} \cdot \mu$, where $\frac{dV_{ch}(y)}{dy}$ is the electrical field along y in the channel, and μ is the effective mobility, we have

$$I_{DS}(y) = \frac{dV_{ch}(y)}{dy} \mu Q W \tag{1.2}$$

Integration of (1.2) in the linear region over channel length L and source-drain voltage V_{DS} results in

$$I_{DS} = \frac{W}{L} \mu C_i (V_{GS} - V_{th} - \frac{V_{DS}}{2}) V_{DS} \tag{1.3}$$

Mobility can be extracted by fitting the I_{DS} vs. V_{GS} curve in the linear region under very small drain voltage, e.g., V_{DS}= -0.1 V. Fig. 1.8 shows the plot for I_{DS} vs. V_{GS} under V_{DS}= -0.1 V in the linear operation regime, and the linear mobility derived from equation (1.3).

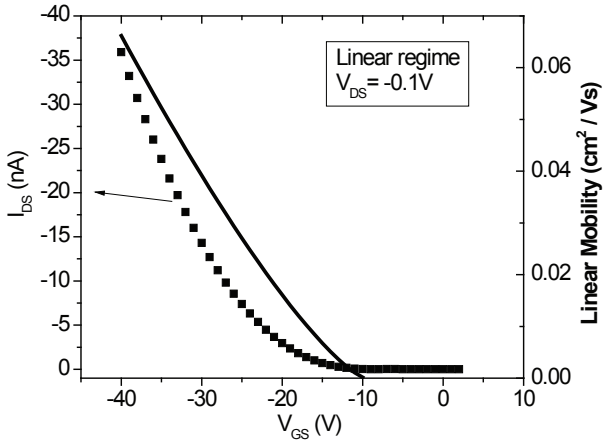

Figure 1.8: Plot for I_{DS} vs. V_{GS} under V_{DS}= -0.1 V in the linear operation regime, and the linear mobility derived from equation 1.3.

As V_{DS} increases, the channel voltage at the drain side will become larger and eventually equal the value of gate voltage, where there will be no induced charge in the channel. This is called "pinch off" point, which happens when V_{ch} at the drain side equals V_{GS} - V_{th}. So the integration of equation (1.2) results in:

$$\int_0^L I_{DS} dy = \int_0^{V_{GS}-V_{th}} W\mu C_i (V_{GS} - V_{th} - V_{ch}) dV_{ch} \tag{1.4}$$

$$I_{DS} = \frac{W}{2L}\mu C_i (V_{GS} - V_{th})^2 \tag{1.5}$$

However, this integration works under the assumption that the mobility is constant and can be taken out of the integration, which is a valid approximation in the linear region but not in the saturation region. So the equation (1.5) only works for single crystalline Si where the mobility is constant and taking square root of both sides of equation (1.5) can be used to derive saturation region mobility through linear curve fitting. In organic systems, such curve fitting cannot be done because as previously noted equation (1.5) is not valid in saturation region. This is confirmed by the nonlinearity in the plot of square root of I_{DS} vs. V_{GS} in Fig. 1.6. Accurate modeling and parameter extraction can be found in chapter 5.

1.3.4 OFET fabrication

Vacuum and solution deposition are the two most common processing methods for OFETs. Conductive layers are commonly deposited by thermal evaporation in vacuum and in some cases coated with conductive ink by spin coating or ink jetting. Small molecule organic semiconductors are most often deposited by vacuum deposition and form polycrystalline structure on substrates. Soluble small molecule semiconductors[26] can also be spin-coated or printed. Polymer organic semiconductors are usually processed from solution using methods mentioned above.

Special considerations are needed in processing and patterning organic materials since they are sensitive to solvents that are used in photolithography and cleaning process. Patterning methods of OFETs include shadow masking, photolithography,[27] and dry printing.[28] This reference [1] covers in detail many aspects of OFETs fabrication and patterning. One of the appendices of the this thesis discusses building two cost-effective laboratory physical vapor deposition and chemical vapor deposition systems for depositing organic semiconductor pentacene and polymer gate dielectric parylene.

1.4 Structure of this thesis

In chapter 1, it is shown that many of the technical obstacles can be approached by studying the interfaces in OFETs. The difficulty of modeling and parameter extraction in disordered systems such as OFETs is also introduced at the end of chapter 1. Chapter 2 focuses on dielectric materials selection including nanocrystals based on barium titanate and high-κ polymer material. Chapter 3 talks about oxygen doping and the illumination effect at the interface between semiconductor and the dielectric layer studied by spectral photocurrent and 1/f noise. Chapter 4 discusses the thiol treatment of the contacts and the performance difference of different thiols; surface probes such as synchrotron X-ray photoemission and photoabsorption spectroscopies are used to probe the difference. Chapter 5 first reviews existing methods for modeling OFETs and the limitations, and then introduces novel methods using photocurrent and spatially resolve photocurrent to model a mobility variant OFET.

Chapter 2

Dielectric Materials

Organic field-effect transistors (OFETs) are potentially competent components for large-area electronics because of their attractive advantages: light weight, cost-effective and large-area processability, flexibility and prospective performance potential. Great effort has been applied to improving device performance, primarily by focusing on enhancing device mobility to increase current capacity and improving subthreshold behavior [19] to reduce the operation voltage.

One approach to improving both figures of merit is to use a high-capacitance gate dielectric, which reduces the operating voltage and increase the mobile charge carrier density for a given gate voltage. Operating at a higher channel charge density improves the effective mobility in OFETs because the the deeper trap states are filled, allowing carrier conduction in states further from the mobility edge.

Several approaches for increasing the gate dielectric capacitance have been proposed including the use of very thin dielectrics [29] [30] [31] [32], deposition of high-κ inorganic dielectrics via sputtering or sol-gel processes followed by high-temperature annealing, [19] [33] [34] [35] [36] and the use of high-κ($<$15) polymer dielectrics [37] [38]. These methods introduce several process complications: thin layers require highly demanding surface conditions, use of inorganic gate dielectrics from solution requires high-temperature, sputtering can require potentially high-cost vacuum processing, and polymeric gate materials offer a limited dielectric constant, respectively.

The method of using the nanoparticle-polymer composite gate dielectrics [39] [40] [41]

[42] [43] appears to have all the advantages simultaneously: much higher dielectric constant compared to polymer dielectrics, low-temperature and large-area processing, and low cost on materials and fabrication, although some of the composites undergo polarization hysteresis [41] [43] and the dielectric constant is limited by the low k polymer and finite solubility of nanocrystals in polymer solution.

In this chapter, I demonstrate the use of nanoscale high-κ materials based on barium titanate (BT) which are normally ferroelectric to be used in applications where their high dielectric constant is desirable but ferroelectric hysteresis is not; I also describe a high-κ relexor ferroelectric polymer material as gate dielectric for OFETs; in both cases, I talk about the surface treatment necessary for semiconductor to form appropriate microstructure that is critical for device function. Dielectric material engineering can not only improve OFETs' performance in terms of operation voltage and mobility, but also provide additional functionalities. The last section of this chapter talks about ferroelectric polymer gate dielectric and its novel applications.

2.1 High-κ dielectrics from self-assembled ceramic nanocrystals

2.1.1 $BaTiO_3$ and $Ba_xSr_{1-x}TiO_3$ nanocrystals

Requirements for integrated electronics are generally towards miniaturization, higher permittivity (dielectric strength), lower loss/leakage.[32] [33] [34] [35] [36] [37] With respect to the family of perovskite materials, it has been predicted and tested that the film thickness or grain size limits applicability in the nanoscale regime.[44] [45] [46] [47] [48] [49] Highly crystalline and aggregate free BT or other perovskite nanocrystals, viewed as "building blocks" for assembly, are strong candidates for materials/ceramics processing in that chemical approaches provide potentially facile and cost efficient fabrication of films.[50] A notable limitation, however, is the trade between the high temperature processing frequently required in order to achieve a desirable level of crystallinity (typically >600°C), versus the unwanted loss of control over particle size and uniformity.[51] Temperatures exceeding 400 °C are generally unfavorable with respect to many substrates and are a red light for any possibility

of adoption by semiconductor industry integrated device manufacturers (IDMs). Furthermore, future technologies that may rely heavily on organic components (plastic electronics, printed or flexible electronics, organic FETs) are seeking thin films of suitable dielectric strength that can be incorporated into entirely solution based or low temperature processing, such as ink jet printing, and can withstand some reasonable level of deformation.[52] [53] The emerging field of nanodielectrics (also called nanometric dielectrics), which specifically deals with the scaling of both ceramic and matrix into the nano regime,[54] [55] [56] impacts research and development from tunable insulators to advanced materials for energy storage.[57] [58] [59] [60]

Aggregate-free, highly crystalline and uniform nanocrystals with narrow size distributions, good size tunability/dispersibility in solvents are strong candidates for solving issues associated with device integration with either conventional semiconductor fabrication or polymer based organic electronics. Our process[61] enables the production of uniform, aggregate-free and highly crystalline $BaTiO_3$ or (Ba,Sr)TiO_3 nanocrystals with high yields (90%) and tunable sizes ranging from about 5 to 100 nm, mainly depending on the type of BaTi metalorganic sources and the type of alcohols used in the synthesis.

$BaTiO_3$ (BT) and (Ba,Sr)TiO_3 (BST) nanocrystals were prepared by reacting 95% ethanol with two different metalorganic sources, barium titanium ethylhexano-isopropoxide, and barium, strontium and titanium isopropoxide, respectively. TEM (Fig. 2.1 (a) and (b)) confirms that the samples consist of discrete $BaTiO_3$ nanocrystals with a relatively narrow size distribution. Nanocrystals of this size have previously been identified as predominantly single crystal, below a natural limit for domain formation. Figure Fig. 2.1 (c) and (d) present typical X-ray diffraction (XRD) patterns of the samples prepared using different barium titanium metalorganic sources. All diffraction peaks can be assigned to the perovskite $BaTiO_3$ phase (JCPDS No. 31-174) or (Ba, Sr)TiO_3 phase without any indication of crystalline byproducts such as $BaCO_3$ or TiO_2. The measurement indicates the exclusive presence of the perovskite phases in high crystallinity and high purity. The sizes of the nanocrystals vary when prepared using different alcohol solvents and different metalorganic sources, as indicated by the extent of the diffraction peak broadening (Fig. 2.1 (c) and (d)), and are consistent with the results based on the TEM observations (Fig. 2.1 (a) and (b)).

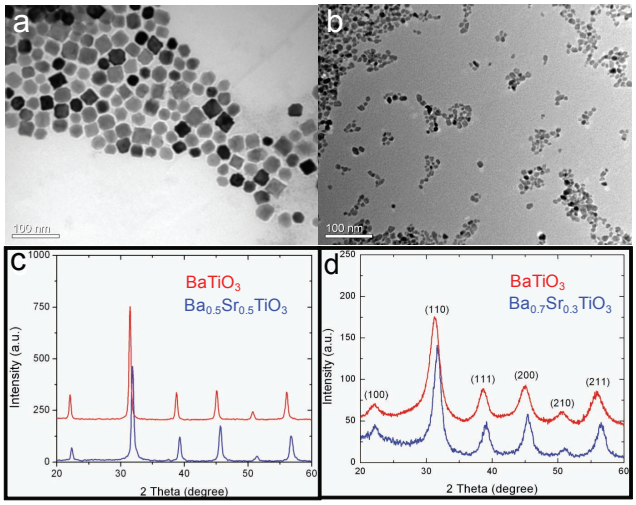

Figure 2.1: TEM images of $BaTiO_3$ nanocrystals synthesized based on a solvothermal process between 95% ethanol and a barium titanium metalorganic source such as (a) barium titanium ethylhexano-isopropoxide and (b) barium and titanium isopropoxide; (c) XRD patterns of $BaTiO_3$ and $Ba_{0.5}Sr_{0.5}TiO_3$ nanocrystals of 25 nm in diameter; (d) XRD patterns of $BaTiO_3$ and $Ba_{0.7}Sr_{0.3}TiO_3$ nanocrystals of 10 nm in diameter.

The individual and highly crystalline BT or BST nanocrystals that result are building blocks that can offer many advantages in low temperature processing (<60°C) of thin films on both rigid substrates (e.g. Si wafer, ITO glass) or flexible substrates (e.g. plastic) by a variety of coating (spin-coating, dip-coating, and cast-coating), spraying and printing techniques. It is challenging to prepare uniform and continuous perovskite oxide thin films with thicknesses down to 100 nm. The problem can be solved by spin coating of a stable nanocrystal suspension. For example, uniform, continuous and crack-free $BaTiO_3$ thin films with variable thickness (50 nm -500 nm thick) were prepared on Si, metal electrode-coated SiO_2/Si, glass substrates or plastic substrates by multiple spin-coating or cast -coating of the nanocrystal suspensions at room temperature followed by baking in air at 60°C to remove residual solvents. The films are optically transparent in the visible range. SEM images (top view and cross-section view, Fig. 2.2) show that the thin films are substantially uniform and continuous while neighboring nanoparticles are touching each other, looking like grains, are readily resolved by the microscope.

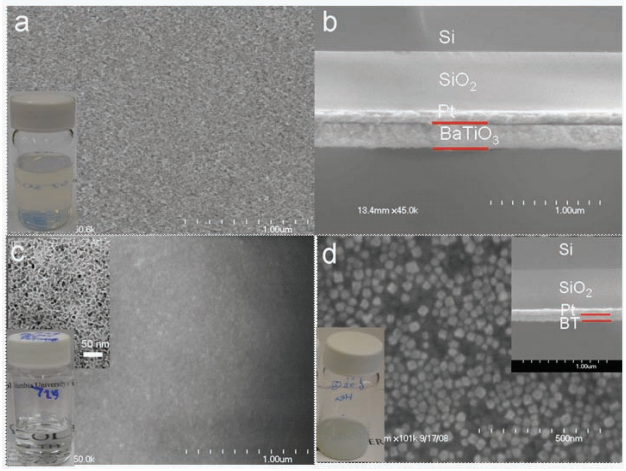

Figure 2.2: (a) SEM images of a $BaTiO_3$ nanocrystal thin film (8nm), top view. (inset) a photo image of a homogeneous ethanol suspension of $BaTiO_3$ nanocrystals (∼20 mg/ml); (b) cross-sectional view of the film; (c) SEM image of poly(alpha-methylstyrene)/$BaTiO_3$ nanocomposite thin film, top view. (inset) a photo image of a transparent poly(a-methyl styrene)/$BaTiO_3$ nanocomposite solution (∼ 20 mg/ml, 8 nm, weight ratio of polymer/$BaTiO_3$ = 1), and a TEM image of the uniform polymer/$BaTiO_3$ nanocomposite; (d) SEM image of poly(alpha-methylstyrene)/$BaTiO_3$ nanocomposite thin film, top view. (inset) a cross-section view of the uniform polymer/$BaTiO_3$ nanocomposite thin film and a photo image of a semitransparent $BaTiO_3$ nanocrystal solution (∼ 20 mg/ml, 25 nm).

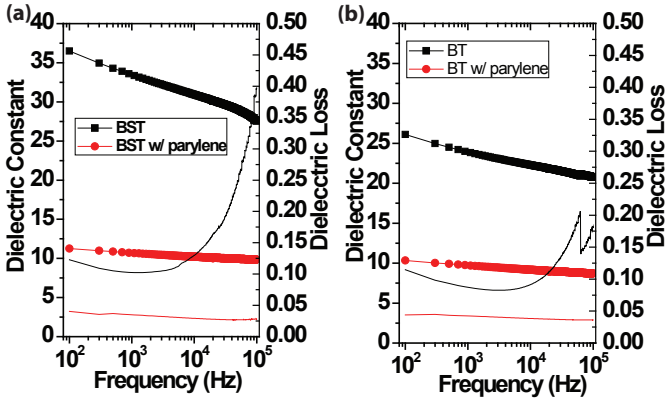

Figure 2.3: Frequency dependence of dielectric constant and dielectric loss for (a) barium strontium titanate (BST) and (b) barium titante (BT) nanocrystal thin films assembled with 8 nm diameter nanocrystals at room temperature.

The combination of high-dielectric-constant nanocrystals with high-dielectric-strength polymer hosts can offer tunable high performance dielectric nanocomposite materials, favorable for capacitor and gate dielectric applications.[62] We prepared uniform polymer/BT nanocomposite thin films based on poly (alpha-methyl styrene)/$BaTiO_3$ with 8 nm (Fig. 2.2(c)) and 25 nm (Fig. 2.2(d)) size particles. The polymer/BT nanocomposite thin film also introduces a smooth, compatible interface that can favor the high-quality crystallization of organic semiconductors such as pentacene. The polymer/BT film is therefore an ideal nanodielectric layer (e.g. high κ) suitable for organic electronics integration, with a direct view towards the fabrication of high performance organic FETs.[53] We verify that homogeneously mixed nanoparticle-polymer composites are attainable, in addition to stepwise laminar composites of layers of particles and polymer.

2.1.2 Dielectric performance - capacitor structure

Dielectric properties were measured on BT and BST nanocrystal thin films sandwiched between two Al electrodes with a crossed area of 1 mm^2. The device consists of 200 nm BT/BST film with 53 nm parylene coating. Parylene is necessary here for the following growth of organic semiconductor (to be covered later) as well as for limiting the leakage. The dielectric measurement was performed on the thin film sandwiched between two crossed

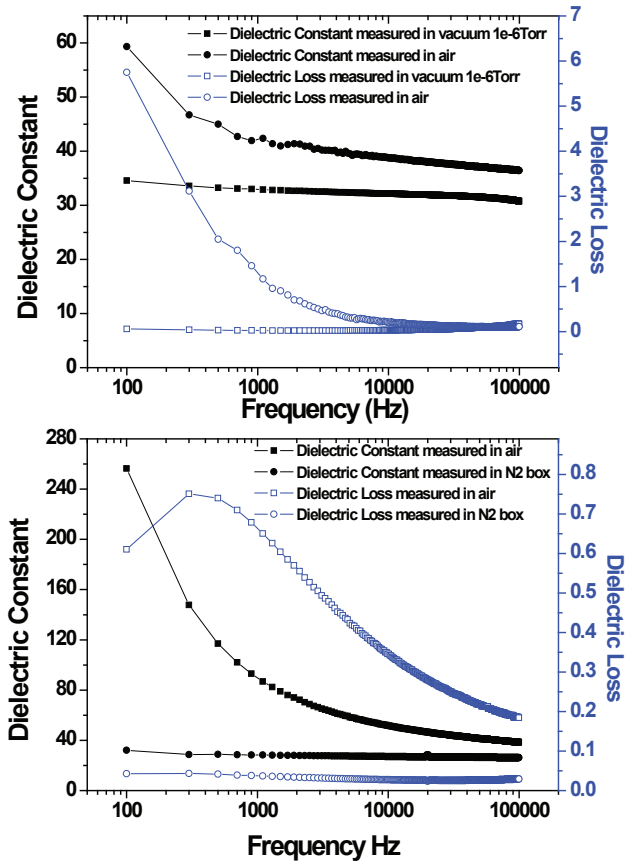

Figure 2.4: Surface moisture effect on the measurement of dielectric constant in BT and BST nanocrystal thin films

Au or Al electrodes with a crossed area of 1 x 1 mm^2. Frequency dependence of the capacitance and dielectric loss were measured using HP4284A LCR meter or HP4156C semiconductor parameter analyzer in the frequency region of 10Hz to 1 MHz. The electric field - polarization hysteresis was measured in air with a Radiant Precision Workstation. All the measurements are done in a N_2 glove box or directly in air on dried samples, since the presence of water which introduces dipoles at the surface of BT particles that affects the frequency dependence of the dielectric response. (Fig.2.4) The dielectric constant for a pure BT film is around 25 on glass and 22 on flexible poly(ethylene naphthalate) (PEN) measured at a frequency of 100 kHz (Fig. 2.3(b)), and the value for parylene coated BT film fell to 10 due to the lower dielectric constant of parylene C ($\sim$3.15). A higher dielectric constant is measured in BST and BST/parylene films (figure 3(a)). The dielectric loss is depressed by the parylene coating while fulfilling the role of limiting leakage current density (9-12 nA/cm^2, measured at 5V dc for a 1x1 mm^2 area). The BT(BST)/parylene thin films also show higher dielectric strength ($\sim$200 V/ m) than pure inorganic thin films (20-100 V/ m).

Previously, a range of values of the dielectric constant of nanotextured BT films have been reported,[45] [46] but is important to note that the contribution of a few percent of larger grains (e.g. $>$ 50 nm) that may be present in samples containing wide size distributions would dramatically affect the dielectric constant. Because no annealing step was undertaken, and the particles and films were characterized as synthesized, we are assured that no large grains are present, and that we are measuring the direct effects of nanocrystals of a specific and narrow size distribution. The dielectric constants of self-assembled nanocrystal thin films as a function of crystal sizes are reported in Table 2.1.

We estimate that inter-crystal voids may take at least 20% volume of a thin film, and therefore suppress the dielectric constant value by predicted linearly proportional factor. A densified film could find higher dielectric constant.[47] For instance, the dielectric constant increases from 47 to 58 (measured at 100 kHz) by filling the voids with amorphous BT materials followed by 60°C baking in air. The dielectric loss remains stable and at a low level under N_2 (tan δ $\sim$0.04 -0.05). Reported loss values of thick BT films prepared by sintering, spark plasma sintering, or r.f. sputtering, are in the range 0.01-0.06.[51] [39] [40] Commer-

Thin film sample	Crystal size (nm)	Dielectric constant (@100kHz)
$BaTiO_3$	8-12	22-25
	25-30	34
$BaTiO_3$/parylene	8-12	10
	25-30	13
$Ba_{0.7}Sr_{0.3}TiO_3$	8-12	27
	25-30	47
$Ba_{0.7}Sr_{0.3}TiO_3$/parylene	8-12	12
	25-30	16

Table 2.1: Dielectric constant of self-assembled nanocrystal thin films as a function of crystal size (film thickness: 200-300 nm)

cially available electrolytic capacitors measured on the same apparatus possess losses in the range 0.04-0.09 (0.1 μF -1 μF). When BT ($BaTiO_3$) nanocrystals (25 nm) are uniformly incorporated into poly (alpha-methyl styrene) (1:1 weight ratio), the dielectric constants show significant increase from $\sim$2.5 for the pure polymer to $\sim$18 for the nanocomposite thin film, and remain stable in the frequency range 100 Hz to 1 MHz.

The critical size limit for free standing (3D) particles has been hotly debated, aided by a range of techniques and probes.[63] [44] [47][49] [64] Suppression of ferroelectricity in free standing particles has been predicted and observed in $PbTiO_3$, $BaTiO_3$ among others.[64] Here we show that BT and BST particles of up to 12 nm in size remain superparaelectric when assembled into films, noting that no grain growth is observed or expected at processing of 60°C. We observe paraelectric behavior over a temperature range of -196°C to 24°C through the distinct observation of no hysteresis in a series of Polarization vs E -Field measurements (Fig. 2.5). The lack of a phase transition between -175°C and 110°C as observed in capacitance measurement (Fig. 2.6) suggests stable and less temperature dependent dielectric constants over a wide temperature range, which would be of benefit for capacitor and gate dielectric applications. Moreover, the high dielectric constant and lack of hysteresis loop in the polarization-electric field plot for the $BaTiO_3$ nanocrystal thin

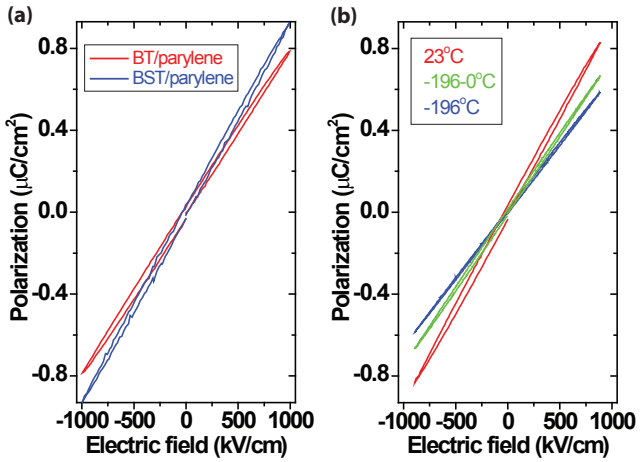

Figure 2.5: Ferroelectric measurements of assembled nanocrystal thin films of BT and BST in Sawyer Tower configuration under conditions of (a) demoisturized films with an evaporated film of parylene, dried at 60°C (b) RT and immersed in liquid N_2 for the BT/parylene thin film.

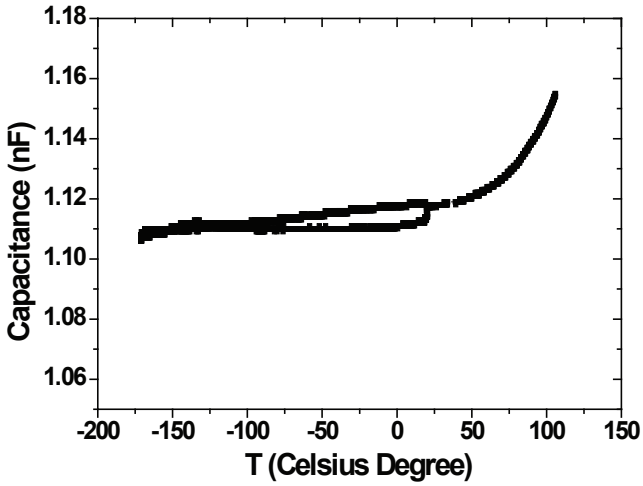

Figure 2.6: Temperature-dependent capacitance measurement in 1^{-6} Torr vacuum for $BaTiO_3$ nanocrystals film.

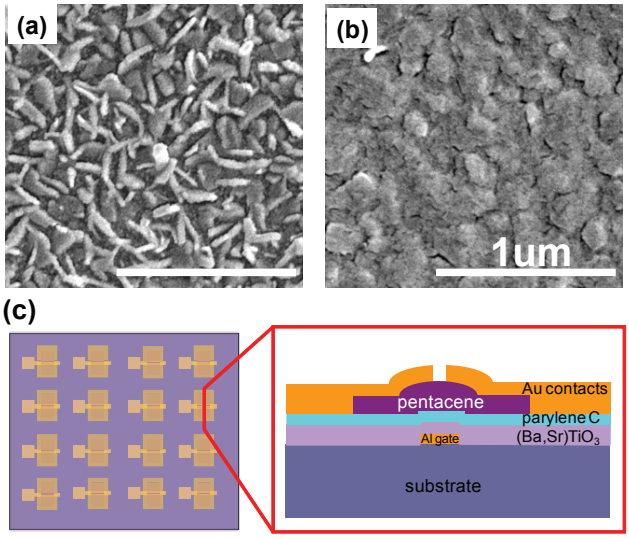

Figure 2.7: SEM images of pentacene grown on (a) bare $BaTiO_3$ thin film and (b) parylene-C coated $BaTiO_3$ thin film. The scale bars in both images are 1 μm. Schematic illustration of pentacene based field-effect transistor configuration (c).

film also show a potential application of the thin film as a high-κ gate dielectric for organic field effect transistors.

2.1.3 Implementation of High-κ nanocrystal dielectrics in OFETs

We fabricated pentacene OFETs with spin-cast high-k barium titanate nanoparticle thin films as the gate dielectric on glass and flexible poly(ethylene naphthalate) (PEN) substrates (Fig. 2.7). In order to solve the incompatibility between inorganic BT (or BST) gate dielectric and the organic semiconductor active layer, a thin layer of parylene-C is evaporated in our customized chemical vapor deposition (CVD) system. The whole fabrication process is operated below 60°C. 25nm of purified pentacene (Luminescence Technology) was deposited and patterned using a shadow mask at the rate of 0.1 A/s with the substrate held at room temperature at a pressure less than 5×10^{-7}Torr. 45nm thick Au source/drain electrodes were deposited through shadow masking. Parylene coating not only helps decrease the surface roughness of nanocrystal thin film, but also provides a favorable surface for the growth of high-quality pentacene. Fig. 2.7 is a comparison of the pentacene grown on bare BT

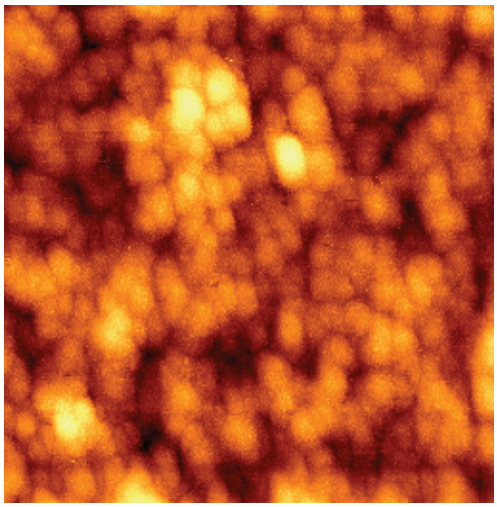

Figure 2.8: Tapping mode AFM image of $BaTiO_3$/parylene The RMS roughness of the bare 8nm BT film is ∼5-6 nm. Parylene coating not only helps decrease the roughness down to 2∼3 nm(with a 30nm parylene coating), but also provides a favorable surface for the growth of high-quality pentacene.

thin film and BT/parylene-C thin film. The pentacene grains fail to form a continuous film on bare $BaTiO_3$ and exhibit a large fraction of vertical grains. No measurable transistor behavior is observed in these samples. Pentacene forms a smooth layer on the parylene-C coated $BaTiO_3$ because of the improved surface roughness (Fig. 2.8). As discussed earlier, the parylene layer also suppresses gate leakage while still allowing for a reasonably high effective dielectric constant.

The I-V characteristics for the OFETs on flexible PEN substrate are shown in Fig. 2.9. With 200nm BST and 53nm parylene-C as the gate dielectric, the effective dielectric constant is 11.3. The device has an on/off ratio 10^4 and mobility 0.25 $cm^2/(Vs)$ in the saturation region fitted using the data from Fig. 2.9(b).

In order to show the superiority of BT/BST gate dielectric, two OFETs samples with 240nm BT coated with 30 nm parylene as gate dielectric and only 250 nm parylene as gate dielectric, respectively, were made under identical conditions (with the same deposition of pentacene). The mobility in linear region (Fig. 2.10) (V_{DS}=-0.1V, V_{GS}=-20V) was enhanced from ∼0.03 $cm^2/(Vs)$ in the parylene control sample to ∼0.35 $cm^2/(Vs)$ in

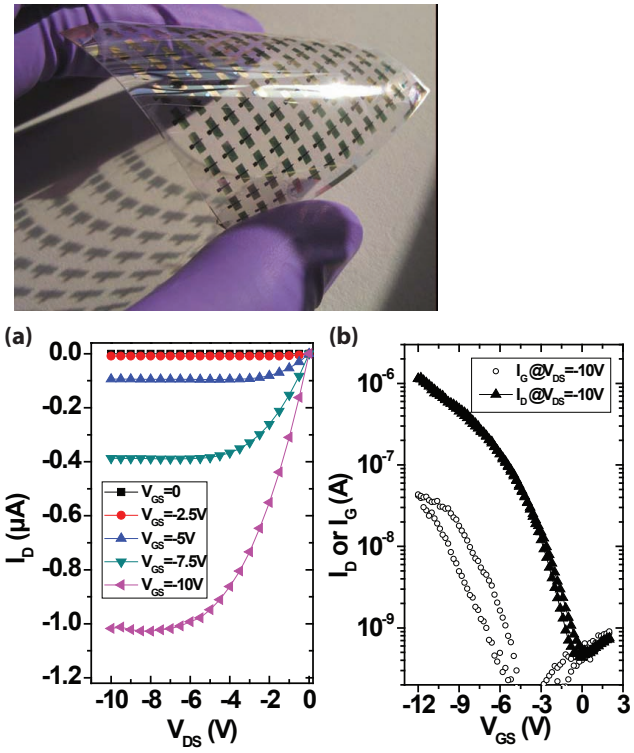

Figure 2.9: Transport characteristics of OFETs on flexible PEN substrate, with 200 nm BST and 53 nm parylene C as the gate dielectric (effective dielectric constant is 11.3). (a) is the drain IV curves under different gate biases. The device has an on/off ratio 10^4 and mobility 0.25 $cm^2/(Vs)$ in the saturation region fitted using the data from (b).

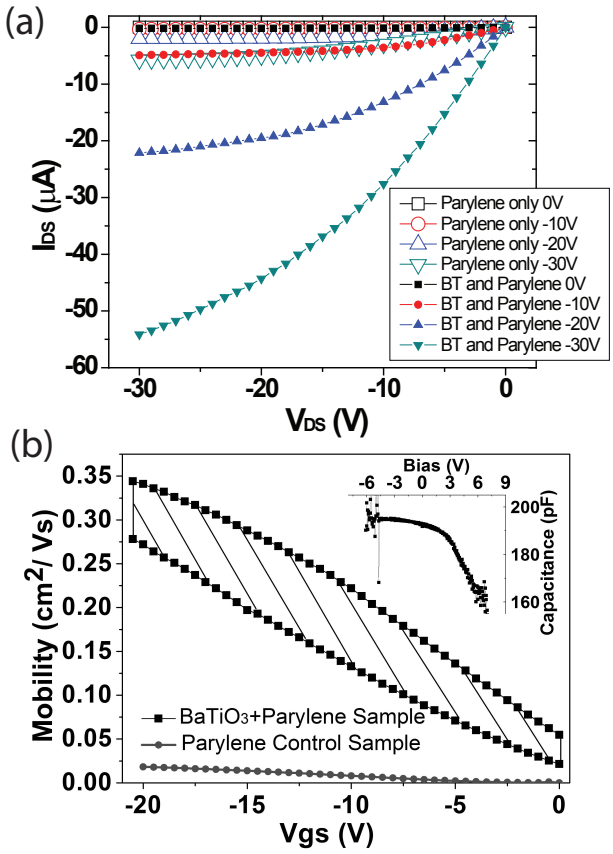

Figure 2.10: (a)Source-drain current of OFETs with parylene only (solid symbols) as gate dielectric and the ones with $BaTiO_3$/parylene (open symbols) as gate dielectric. (b)Linear mobility in OFETs with parylene only (dots) as gate dielectric and the ones with $BaTiO_3$/parylene (squares) as gate dielectric.

BT/parylene sample, attributed to increased concentration of accumulated carriers in the latter case. While the parylene control sample generates 0.22C/cm^2 under V_{GS}=-20V, the BT/parylene sample generates 0.72C/cm^2 under V_{GS}=-20V.

2.2 P(VDF-TrFE-CFE) terpolymer

Poly(vinylidene fluoride-trifluoroethylene) (PVDF) is a ferroelectric, piezoelectric and pyroelectric [65] polymer. Defect modification through chemical modification and electron bombardment of PVDF converts the normally ferroelectric material into a ferroelectric relaxor with high dielectric constant.[3] Poly(vinylidene fluoride-trifluoroethylene-chlorofluoroethylene) [P(VDF-TrFE-CFE)] and Poly(vinylidene fluoride-trifluoroethylene-chlorotrifluoroethylene) [P(VDF-TrFE-CTFE)] are two kinds of chemically modified materials, which exhibit a slim polarization hysteresis loop.(Fig. 2.11) Typically the random of incorporation of CTFE ter-monomers into polymer chains causes disordering of the ferroelectric phase. Inclusion of these defects randomizes the inter- and intra-chain dipolar coupling and eliminates the barrier in the transformation between different molecular conformations, resulting a relaxor erroelectric behavior.[66]

The dielectric constant and dielectric loss as a function of frequencies are shown in Fig. 2.12. Because of its high dielectric constant, P(VDF-TrFE-CFE) is also used as gate dielectric in low operation voltage OFETs. (Fig. 2.13) P(VDF-TrFE-CFE) terpolymer also exhibits a high electrostrictive strain at room temperature and has applications in actuators. See appendix.

2.3 Ferroelectric functional dielectric materials

2.3.1 Ferroelectric P(VDF-TrFE) and its application in OFETs

Poly(vinylidene fluoride-trifluoroethylene) [P(VDF-TrFE)] copolymer is one of the most common ferroelectric polymers that can be used as non-volatile memory in flexible electronics. Many memory devices based on OFETs with ferroelectric dielectric has been demonstrated. [67] [68] [69] [70] [71] In our proposed concept, an OFET includes a ferroelectric

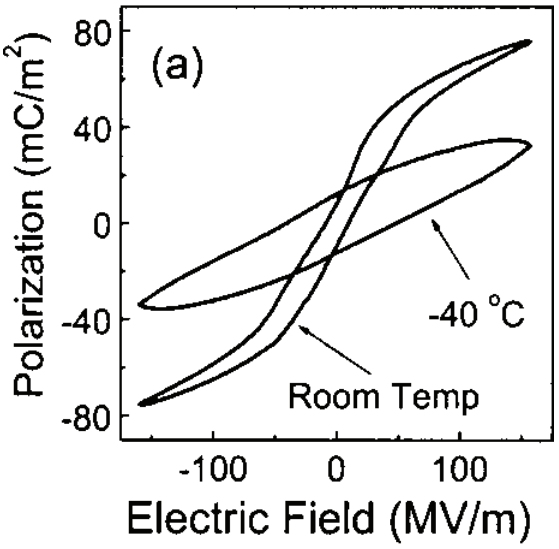

Figure 2.11: Hysteresis loop measured at two temperatures.[3]

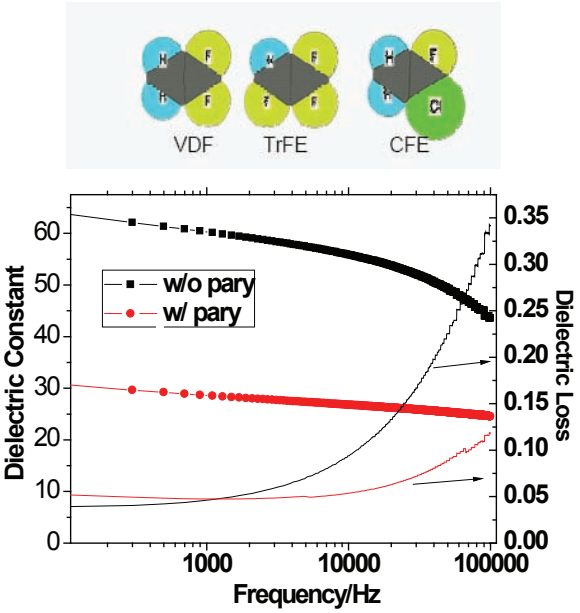

Figure 2.12: Frequency dependence of dielectric constant and dielectric loss for P(VDF-TrFE-CFE) terpolymer film.

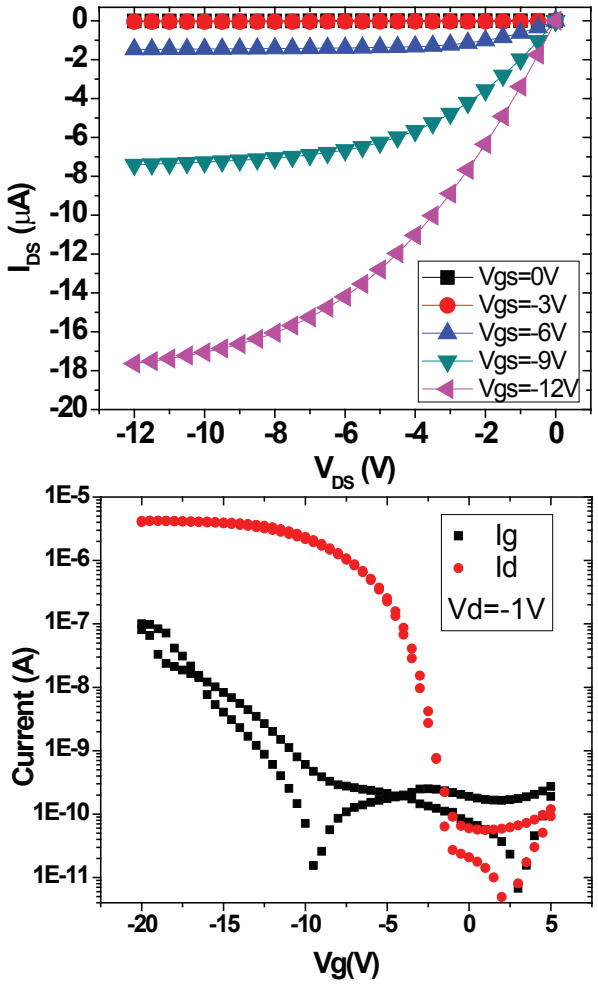

Figure 2.13: Transport curves for OFETs based on P(VDF-TrFE-CFE)(180 nm)/parylene (10nm) composite dielectric. W/L=860μm/50μm; layered dielectric: κ=31; mobility$\sim$1cm^2/Vs

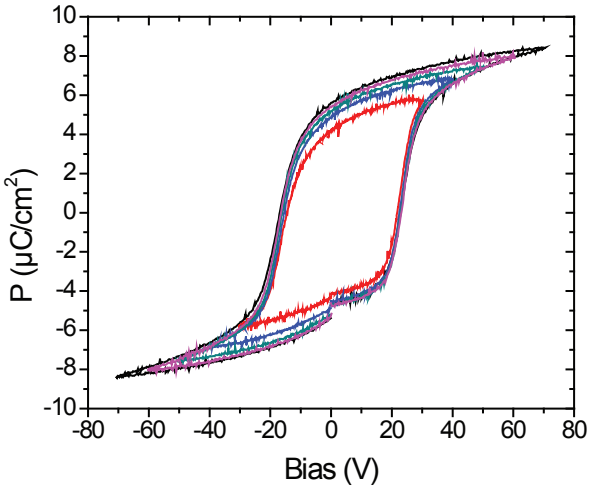

Figure 2.14: The polarization-voltage (P-V) hysteresis loops are measured in air at room temperature. This particular device shows a saturation polarization of 8.3 μC/cm^2 and a remanent polarization of 5.4 μC/cm^2 with a coercive voltage of approximately 20 V.

gate dielectric permitting electrical reprogramming, such as to implement an electrically re-programmable array logic (PAL) or a field-programmable gate array (FPGA). Since an OFET with a ferroelectric gate dielectric can be switched between enhancement mode (V_{th} <0 V) and depletion mode (V_{th} >0 V) by external field, multiple such units can constitute functional devices such as "NOT," "AND," "OR," "NAND," and "NOR," and such functional devices are multiple-time programmable and switchable.

In P(VDF-TrFE) most of the electrons are attracted to the fluorine side of the chain and a polarization persists after the electric field is removed. Similar to PVDF, P(VDF-TrFE) has four known phases; phase I (β), phase II (α), phase III (γ) and phase IV (σ). The β phase is the all-trans zig-zag configuration, which generates the largest polarization.[72] The polarization-voltage (P-V) hysteresis loops are measured in air at room temperature and shown in Fig. 2.14. This particular device shows a saturation polarization of 8.3 μC/cm^2 and a remanent polarization of 5.4 μC/cm^2 with a coercive voltage of approximately 20 V. Fig. 2.15 shows the capacitance under different bias with a characteristic butterfly shape.

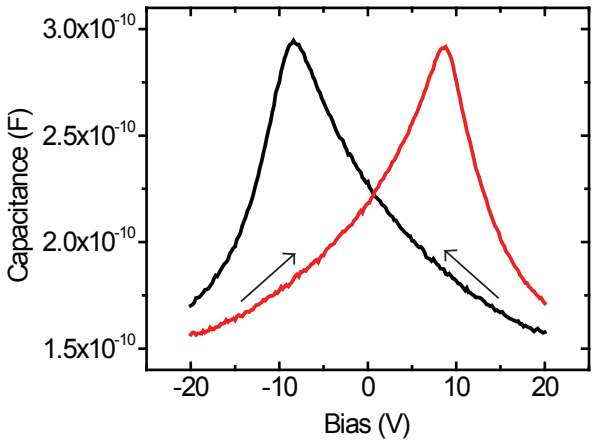

Figure 2.15: The capacitance measurement under different bias with a characteristic butterfly shape

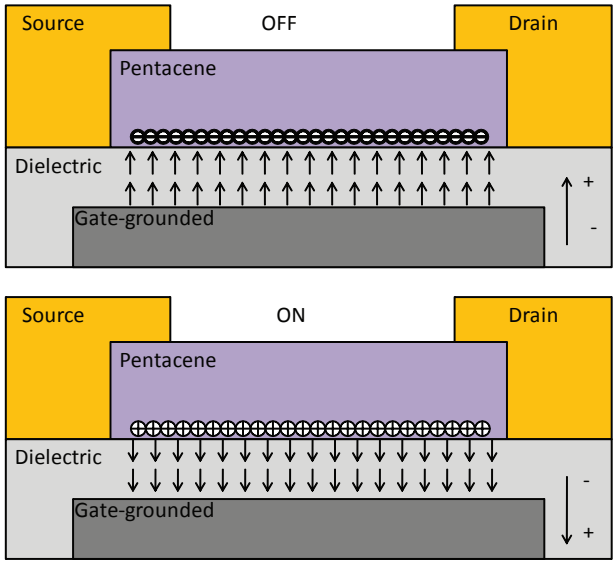

Figure 2.16: Schematic of the operation principle of OFETs with ferroelectric gate dielectric. The arrows indicate the two remnant states of polarization in the ferroelectric layer.

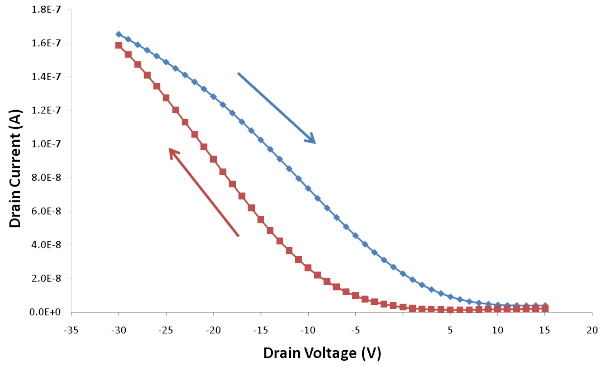

Figure 2.17: A fabricated pentacene OFET with ferroelectric dielectric. 30nm pentacene was directly deposited on P(VDF-TrFE) without any surface treatment prior to the deposition. The arrows indicate the directions of voltage ramping.

The operation of an OFET with ferroelectric gate dielectric can be explained as in Fig. 2.16. The ferroelectric layer can adopt either of the two stable polarization states under no bias. Depending on the orientation of the polarization, positive or negative charges can be induced in the semiconductor close to the semiconductor-dielectric interface. For pentacene, only positive charges are conductive and thus the device is on when the remanent polarization from P(VDF-TrFE) induces positive charges in the channel. This switching characteristic shows a hysteresis in a drain current - gate voltage sweep, with the edges of the switching on either side of the 0 V. Switching from one polarization state to another can be realized by applying a large enough gate voltage [larger than the coercive voltage of P(VDF-TrFE)] and thus both enhancement mode and depletion mode transistor can be realized on the same device. Fig. 2.17 is the IV curve of a fabricated device.

2.3.2 A few words about P(VDF-TrFE) processing

P(VDF-TrFE) film is usually solution deposited by spin coating. 6-12% P(VDF-TrFE) in 2-butanone or Dimethylformamide (DMF) solution is span at the speed of 1000-3000 rpm. As a reference, a 8% soution that is span coated at 1500 rpm and below usually has a yield of 90% of non-leaky devices given the heating and cooling processes are well controled. A very helpful optimization recipe can be found in this reference.[72]

Slow cooling is necessary to increase the crystallinity of the film, and also improves the surface morphology. Generally the P(VDF-TrFE) film surface is rough (roughness root mean square $>$ 7 nm[73]) because the random recrystallization process happened during the cooling.

The ferroelectric performance is not sensitive to heating methods. We have tried vacuum oven, air oven, hot plate, and hot plate in N_2 environment, and the ferroelectric performance is similar among those films.

Moisture plays an important role in film quality. The films come out much better if the P(VDF-TrFE) pellets are baked at 100°C for 10 minutes before being dissolved and the glass substrate are baked at 120°C for 10 minutes before spin coating. Removal of moisture also increases the adhesion of the copolymer film on substrate.

2.4 The dielectric-semiconductor interface - a brief introduction

The grain size and grain boundaries are not necessarily critical aspects for transport in pentacene OFETs, and thus the crystal structures especially characterized on a thick film of pentacene can not be linked directly to device performance. However, the stacking of molecules for the first several layers of pentacene on a dielectric surface is essential for high performance. Pentacene tends to form the closely packed thin film phase structure on a low energy surface and tends to lie down on a high energy surface. Much work has done to achieve favorable morphology for pentacene growth and attentions have been paid to intentionally and unintentionally induced dipole layer at the dielectric-semiconductor interface by the usage of self assembled monolayer surface treatment.[4] [5] [74] [75] [76] [77] Unfortunately many of them do not give a clear picture of how the dipoles change the threshold voltage for as large as 40 V. At the beginning of next chapter, this problem will be addressed.

2.5 Conclusion

In this chapter, I have demonstrated that nanoscale high-κ materials which are normally ferroelectric are used in applications where their high dielectric constant is desirable but ferroelectric hysteresis is not. I have shown a method of surface treatment method to solve the incompatibility between organic semiconductors and inorganic dielectrics. By using the layered dielectric material, OFETs with enhanced mobility and reduced operation voltage have been fabricated. I have also introduced a relaxor ferroelectric polymer for the use as high-κ dielectrics. OFETs with a ferroelectric gate dielectric permits electrical reprogramming, such as to implement an electrically re-programmable array logic.

Chapter 3

The Dielectric-Semiconductor Interface

Dielectric-semiconductor interface is the most important interface in OFETs operation. The quality of this interface and the first couple of molecular layers of the semiconductor next to the interface determine the overall quality of the device.

Self-assembled monolayer (SAM) treatment of the dielectric has been used to improve the morphology of subsequently deposited organic semiconductor. The dipoles within the SAM, however, dramatically change the electrical performance in terms of threshold voltage and mobility. The first part of this chapter reviews the SAM treatment and explains why there is a substantial change in threshold voltage.

OFETs are sensitive to their environment and can be degraded by exposure to reactive materials both during and after fabrication. In particular, exposure of the gate dielectric to oxidizing agents prior to depositing the semiconductor can introduce a fixed charge at the gate dielectric interface and shift the threshold voltage of OFETs [6]. The electrical performance difference have been attributed to morphology, dipole layer and charge transfer. In the second part of this chapter, this problem is studied using spectral photocurrent and $1/f$ noise measurement by comparing OFETs whose polymer gate dielectric is exposed to UV ozone prior to semiconductor deposition with control OFETs whose semiconductor/dielectric interface is produced in a nearly oxygen-free environment.

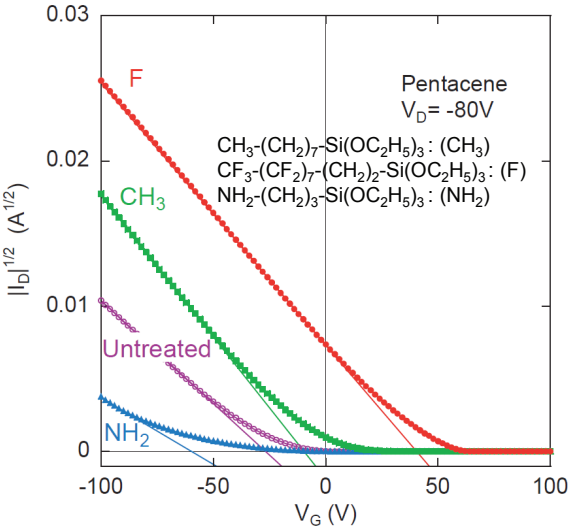

Figure 3.1: Taken from [4]. Square root of drain current vs. gate bias of pentacene OFETs with organosilane SAMs treated dielectric. Mobility has also improved in F-SAM treated sample seen from the slope of the curve.

3.1 Self-assembled monolayer treatment of the dielectric

Studies have shown that surface treatment of the oxide dielectric surface before depositing semiconductor using organosilane self-assembled monolayers (SAMs) can modulate the carrier density and change the threshold voltage. Many studies mentioned at the end of last chapter have demonstrated the ability of changing threshold voltage by applying organosilane SAMs with different dipoles (Fig. 3.1, taken from [4]). Particularly, SAMs with a dipole moment facing down to the dielectric surface shift the threshold voltage positively with a difference as large as many tens of volts, as seen in Fig. 3.1.

Fig. 3.2 explains how such a threshold voltage shift happens. The F-SAM dipole layer induces polarization across the dielectric layer. This is identical to applying a negative gate voltage to polarize the dielectric. If this pre-bias polarization is large enough, the threshold voltage can be shifted over 0 V and the transistor is in depletion operation mode. The next question is how large the effective gate bias is when a layer of dipole molecules with the dipole moment of 1-2 D (usually the case for SAM treatment) is deposited on the dielectric

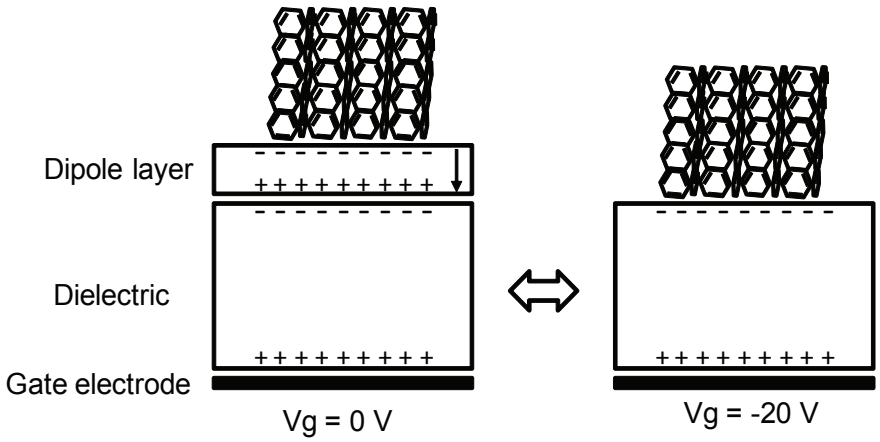

Figure 3.2: The F-SAM dipole layer on top of dielectric induces polarization across the dielectric layer. This is identical to applying a negative gate voltage to polarize the dielectric.

surface.

The dipole molecule layer change the surface potential by:

$$\Delta\phi = N(\frac{\mu_{mol,\perp}}{\epsilon_0\epsilon}) \tag{3.1}$$

where $\Delta\phi$ is the surface potential shift due to a dipole layer, N is the areal density of molecules, $\mu_{mol,\perp}$ is the SAM molecule dipole moment projected to the surface normal direction, ϵ_0 is the vacuum permitivity and ϵ is the relative dielectric constant of the thiol molecules. If we compare the CF_3-$(CF(CF_2)_7)_7$-$(CH_2)_2$-$Si(OC_2H_5)_3$ SAM with a dipole moment of -2.20 D and the CH_3-$(CH_2)_7$-$Si(OC_2H_5)_3$ SAM with a dipole moment of 0.83 D, the surface potential difference between them according to (3.1) should be 0.4 - 1.1 V, assuming N is about 1-2$\times$ 10^{14} cm^2, and for both SAMs ϵ is 2-3.[4]

The dielectric layer and the SAM layer can be seen as two capacitors in series (Fig. 3.3), which means the interface charges $Q_1 = Q_2$. Since $Q = CV$ we have:

$$C_1 \cdot \phi_1 = C_2 \cdot \phi_2 \tag{3.2}$$

$$\frac{\epsilon_0\epsilon_1}{d_1} \cdot N(\frac{\mu_{mol,\perp}}{\epsilon_0\epsilon}) = \frac{\epsilon_0\epsilon_2}{d_2} \cdot \phi_2 \tag{3.3}$$

$$N\frac{\mu_{mol,\perp}}{d_1} = \frac{\epsilon_0\epsilon_2}{d_2} \cdot \phi_2 \tag{3.4}$$

where d_1 and d_2 are the thickness of the SAM molecule layer ($\sim$ 1 nm) and the thickness of

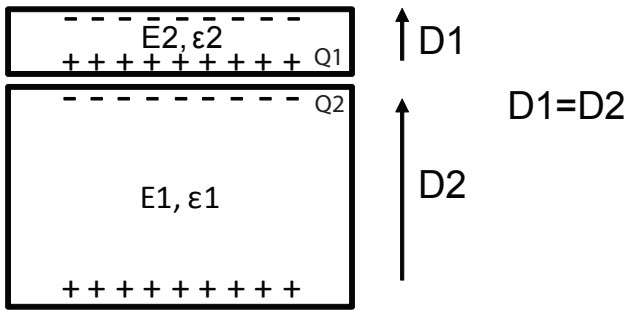

Figure 3.3: The dipole layer induces polarization in the dielectric layer. The system can be seen as two capacitors in series and $Q_1 = Q_2$. Boundary conditions also require the electric displacement field is continuous across the interface at the direction perpendicular to the interface plane $D_1 = D_2$. These two conditions are consistent.

the dielectric layer, respectively. The dielectric constant of the SiO_2 dielectric is 3.9 and its thickness is 400 nm. So the difference of identical gate voltages from F-SAM and CH_3-SAM is around 116 - 232 V, which is three to seven folds threshold shift measured. Considering the approximations and rough estimation of molecular stacking density and stacking angle (perpendicular stacking assumed here), this is reasonable. Another identical calculation to the above one is:

$$\frac{\epsilon_0\epsilon_1}{d_1} \cdot \phi_1 = \frac{\epsilon_0\epsilon_2}{d_2} \cdot \phi_2 \tag{3.5}$$

$$\epsilon_1 \frac{\phi_1}{d_1} = \epsilon_2 \frac{\phi_2}{d_2} \tag{3.6}$$

which means:

$$\epsilon_1 E_1 = \epsilon_2 E_2 \tag{3.7}$$

$$D_1 = D_2 \tag{3.8}$$

where E and D are the electrical field and electric displacement field, respectively. This is consistent with boundary conditions which require electric displacement field is continuous across the interface at the direction perpendicular to the interface plane (Fig. 3.3).

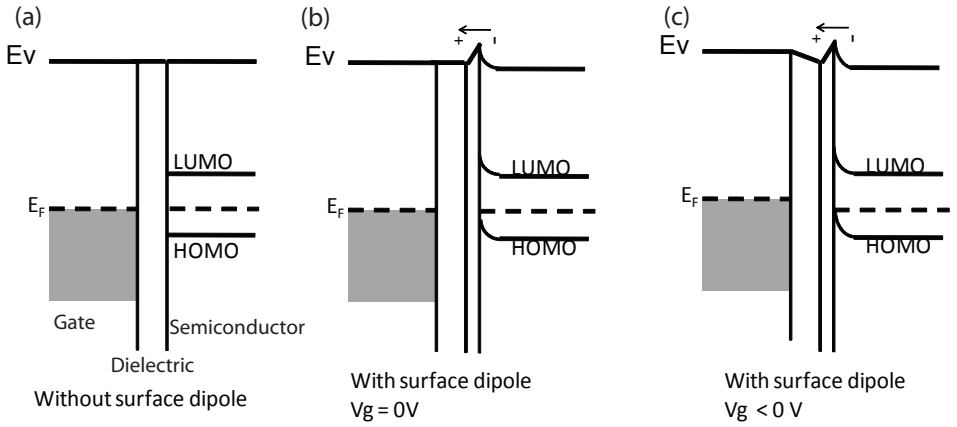

Figure 3.4: The bands diagram for the SAM treated metal-oxide-semiconductor structure, adapted from reference [5].

Fig. 3.4 shows the band diagram for the SAM treated metal-oxide-semiconductor structure, adapted from reference [5]. In (a), we assume that there is no band bending when pentacene is deposited on SiO_2 dielectric. This assumption is rough but does not keep us from understanding the effect of dipole SAM. With a F-SAM on the dielectric surface, the surface potential is modified and the vacuum level tilts up. Correspondingly the HOMO LUMO bands also bend at the interface. This pulls the HOMO closer to Fermi and holes are populated. This is identical to applying a negative gate voltage. The band bending is small but the charges are exponentially proportional to the energy distance between HOMO and Fermi, and a small band bending will induce a large amount of charges in the channel.

3.2 UV-ozone treatment of the dielectric

UV ozone treatment of the dielectric layer, which is sometimes used for cleaning processes, shifts the threshold voltage positively and increases the channel conductivity, and thus changes the OFET operation from enhancement mode to depletion mode. Fig. 3.5 shows the electrical measurements of a UV ozone treated OFET and an air free (no air exposure during fabrication) OFET. The lower part is the study [6] of how UV ozone treatment time affects the threshold voltage. It shows that the mobility also changes: μ=0.41, 0.23, 0.46, 0.48 and 0.71 cm^2/Vs in the control, 30 s, 1 min, 2 min and 5 min treated devices, respectively.

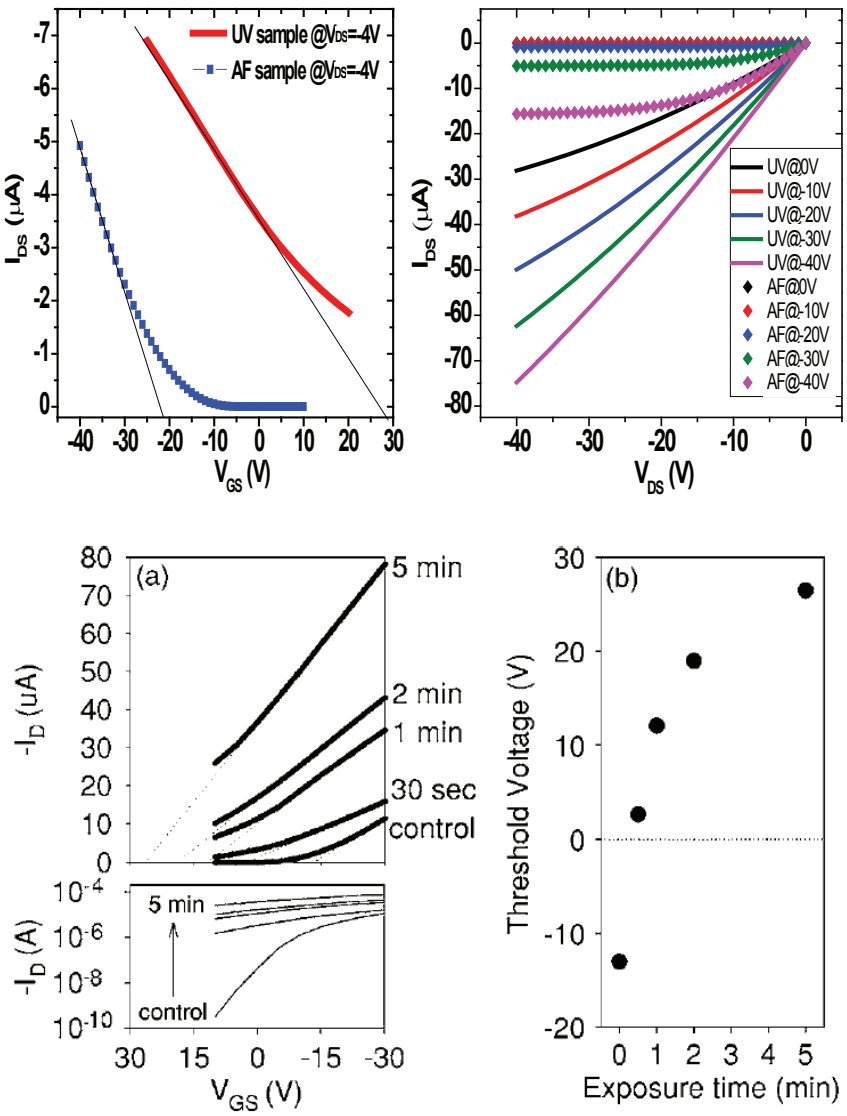

Figure 3.5: Upper: Electrical measurement and characteristics comparison of UV treated sample and air free sample in this work; Lower: threshold shift vs. UV ozone time taken from reference[6]

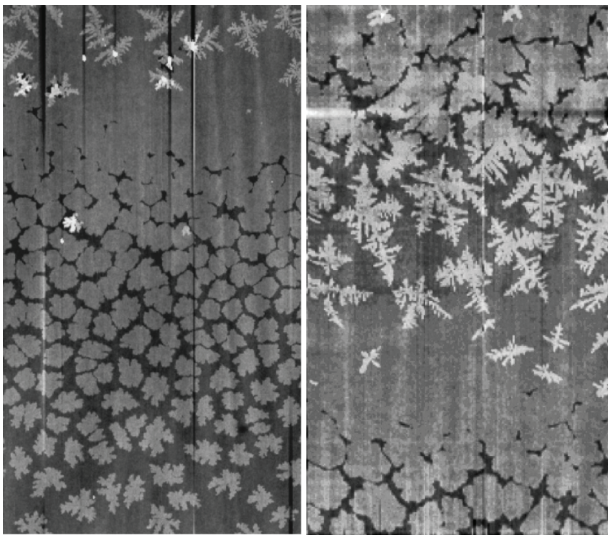

Figure 3.6: Although the microstructure of pentacene grown on hydrogen and oxygen plasma treated dielectric surface is very similar, the threshold voltage has an 80 V difference. From reference[7]

The gate-bias dependent mobility seen in the control device disappears in the UV treated ones under high gate bias. Studies have attributed these changes to morphology change,[78] dipole contribution,[79] and electron transfer from semiconductor to the dielectric surface.[7]

First of all, the electrical performance difference is not a morphological effect. Fig. 3.6 from reference [7] shows that although the microstructure of pentacene grown on hydrogen and oxygen plasma treated dielectric surface is very similar, the threshold voltage has a 80 V difference. AFM study on pentacene grown on control parylene and UV-ozone treated parylene surface shows similar results: the two have similar morphology but different threshold voltage (Fig. 3.7). In Fig. 3.8 near-edge x-ray absorption fine structure (NEXAFS) study on monolayer pentacene deposited on both surfaces also confirms that the pentacene has the same standing-up structure in the two cases, because of the change of π^* intensity when switching the polarization (see chapter 4). The peak around 285 eV in p polarization curves are from the underneath parylene.

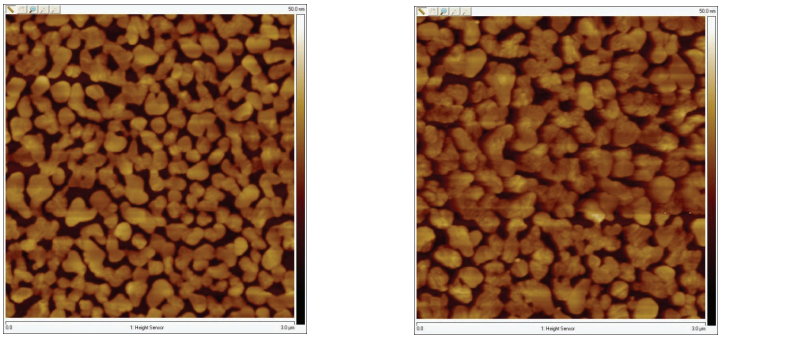

Figure 3.7: AFM of 10 nm pentacene grown on control parylene and UV-ozone treated parylene surface.

X-ray photoelectron spectroscopy (XPS) (Fig. 3.9) shows that oxygen is presented in the UV treated parylene surface while the control parylene does not show any. It is proposed that [7] oxygen plasma created electroactive centers such as radicals that act as electron acceptors. Such electron trapping centers may include -OH, -$O^{\bullet}$, and -O-$O^{\bullet}$. The radicals can trap electrons from pentacene and release hole carriers in the channel which contribute to the channel conductivity. The study relates surface treatment and the residual carriers in semiconductor which is measured by independent 4-probe measurement. It is found out that Ar and O_2 plasma treatment, which generates mainly -$O^{\bullet}$ and -O-$O^{\bullet}$ radicals increases residual carrier density by two orders of magnitude compared to H_2 plasma treatment, which generates mainly $C^{\bullet}$ and C-H, or without any treatment. Fig. 3.10 summaries the surface defects generated by various plasma treatment taken from reference[7].

Interaction with the recombination centers is different from interaction with dipole layer mentioned previously. Dipole layer can trap and release carriers, and the carriers are not "sticky." The recombination centers capture electrons from semiconductor and release holes to the channel. This charge transfer is possibly permanent; it results in much larger conductance in the channel and rather straight transconductance curve in p-type transistors. Dipole interaction usually does not generate a large hysteresis in the transconductance curve

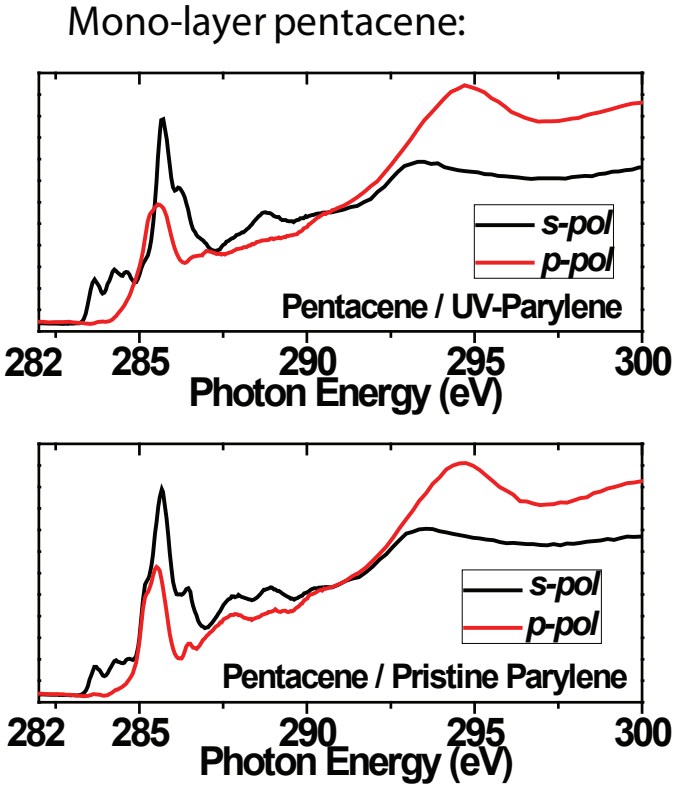

Figure 3.8: NEXAFS study on monolayer pentacene deposited on both surfaces also confirms that the pentacene has the same standing-up structure in the two cases, because of the change of π^* intensity when switching the polarization (see chapter 4). The peak around 285 eV in p polarization curves are from the underneath parylene.

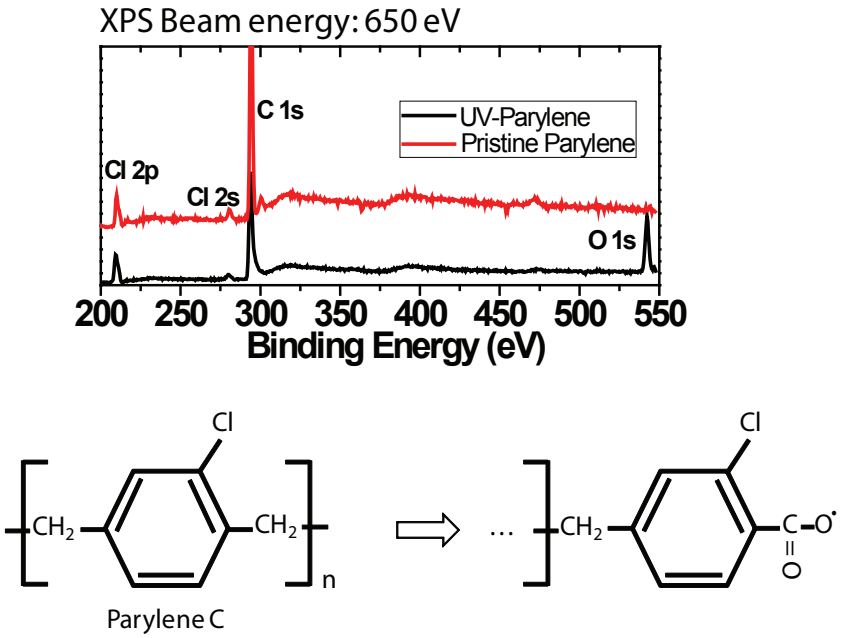

Figure 3.9: X-ray photoelectron spectroscopy (XPS) shows that oxygen is presented in the UV treated parylene surface while the control parylene does not show any.

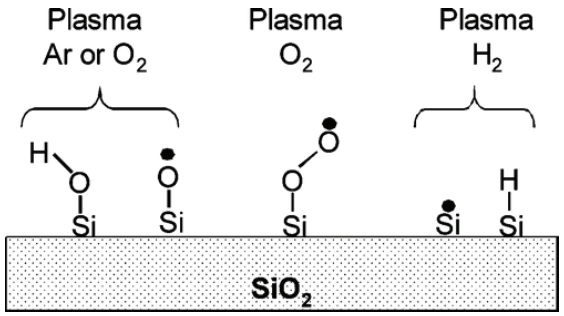

Figure 3.10: Defects on oxide surface with various plasma treatment. Taken from reference[7]

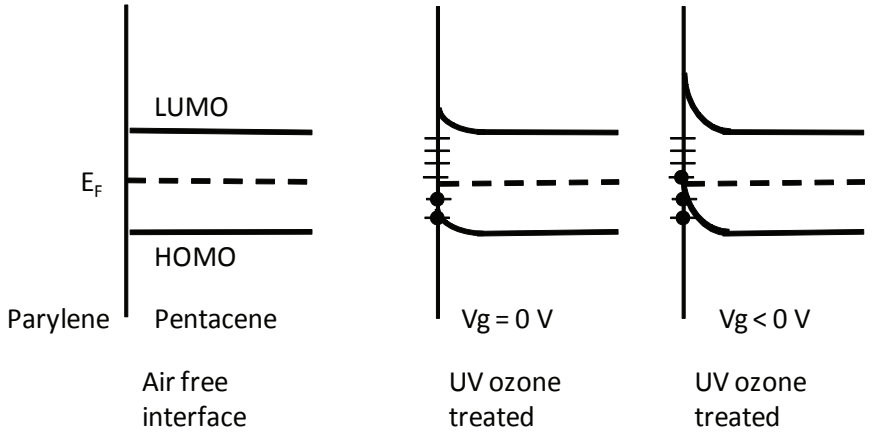

Figure 3.11: Recombination centers at the interface extract electrons from pentacene and release holes to the channel. The trapped electrons shift the threshold voltage positively. Hysteresis in the transconductance sweep can also be explained based on this diagram. When a negative gate bias is applied, further band bending fills more traps and thus more holes are released into the channel; when the band sweeps back, the trapped electrons are "sticky" and will not fall back to the HOMO immediately.

while recombination centers induce very large hysteresis. A possible band diagram is presented in Fig. 3.11. The trapped electrons shift the threshold voltage positively. Hysteresis in transconductance sweep can also be explained based on this diagram. When a negative gate bias is applied, further band bending fills more traps and thus more holes are released into the channel; when the band sweeps back, the trapped electrons are "sticky" and will not fall back the HOMO immediately.

3.3 UV-ozone treatment of the dielectric studied by spectral photocurrent

The spectrally resolved photocurrent response is a nondestructive method to probe the energy states in OFETs by exciting pentacene molecules at different energy levels and observing their contribution to the device current [80] [81] [82]. The photocurrent also provides useful information on carrier mobility [83], the presence of oxygen-induced states [80], and the location of states in the HOMO-LUMO gap [81] of pentacene. As a continuation of the

work by Wang *et al.* [82], we have applied photocurrent spectroscopy to study the interface states introduced by UV-ozone treatment of the gate dielectric and compared this to devices produced without any air exposure during their fabrication process. Our studies shows that the acceptor-like interface trap states in UV-treated sample can effectively increase the photocurrent, especially when the incident photons have energies larger than the HOMO-LUMO gap of pentacene. We attribute this to the improved exciton dissociation process due to electron-withdrawing traps.

3.3.1 Spectral photocurrent setup and sample preparation

Pentacene OFETs with a parylene-C gate dielectric were fabricated on glass substrates using a bottom-gate, top-contact structure. The gate, semiconductor, and source/drain contacts were patterned using shadow masking. Thermal evaporation of Al gate electrodes was followed by the deposition of a blanket layer of parylene as a gate dielectric in a custom chemical vapor deposition (CVD) system. 25 nm of pentacene was vacuum evaporated at the rate of $0.1 \sim 0.2$ A/s with substrate held at room temperature at a pressure $< 5\times10^{-7}$ Torr. Au source and drain contacts were then thermally evaporated. All of the evaporation and CVD systems are attached to the same glovebox cluster which is continuously scrubbed for oxygen and water (< 0.1 ppm for both). This allows fabrication of OFETs without exposure to oxygen or water vapor. As a comparison, the parylene dielectric on another sample set was both exposed to air and treated with UV-ozone for 10 minutes prior to the pentacene deposition. An air-free and a UV-treated sample were placed into the pentacene evaporator at the same time to avoid any process variation, and more than 100 devices are fabricated on each sample.

With transistors biased using a Keithley 2602 two-channel source/measure unit, the photocurrent was generated using a monochromated Xe arc light source, and the photocurrent was measured using a Signal Recovery 7265 lock-in amplifier with frequency locked to 171 Hz while the arc lamp was mechanically chopped. A schematic of measurement setup is shown in Fig. 3.12. The photocurrent was linearly normalized with the illumination intensity spectrum measured using a calibrated Si photodiode. We independently confirmed that the photocurrent response is linear with the illumination intensity at the applied intensity

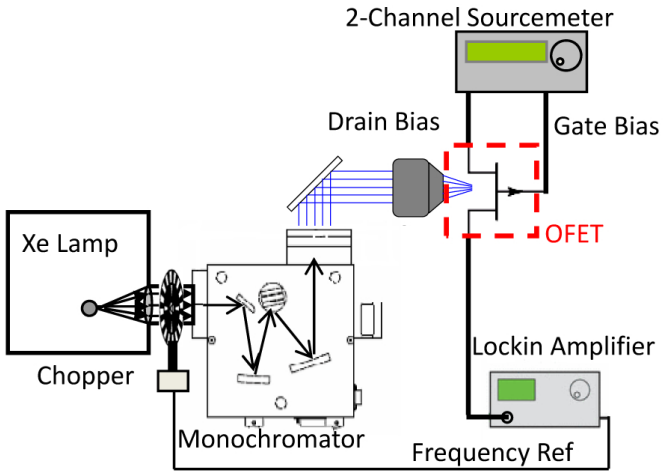

Figure 3.12: Schematics of photocurrent measurement setup.

levels (approximately) using single color LED illumination.

3.3.2 Spectral photocurrent measurements

Fig. 3.13 is wavelength dependent photocurrent spectrum of a control sample and UV treated sample taken with 2 nm wavelength steps at different gate biases. We first notice that generally the UV treated sample has much higher photocurrent than the air free samples. As we later show in chapter 5, photocurrent is proportional to the product of photo-generated carrier density, mobility and bias. With identical or similar mobility and bias in the two cases, we think that the higher photoresponse from UV sample is due to fact that the oxygen radials form a layer of electron trapping sites at the interface. In the air free sample, photons excite pentacene molecule and form excitons; the exitons dissociate into electron and holes under the effect of electrical field. In the UV treated sample, the trapping of electrons on the interfacial states strongly facilitate the electron-hole dissociation and more holes are released into conduction. Within each sample, the photocurrent intensity also increases with decreasing gate biases with the peaks positions and their shapes unchanged. This increased photocurrent is due to increased mobility (see chapter 5) with decreased more negative gate bias. There are two manifolds of peaks in the range of 520 nm - 680 nm and 350 nm - 480 nm, respectively. Four major peaks (544 nm, 588 nm, 630 nm, 668 nm) are attributed to the Davydov doublet of the 0-0 and 0-1 band transitions,[84]

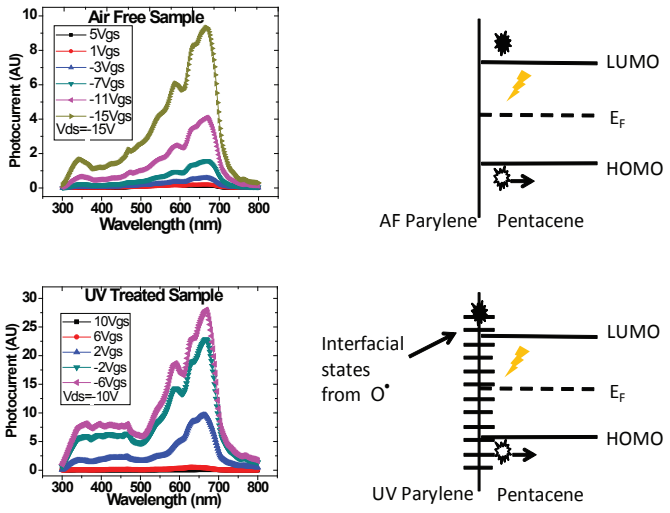

Figure 3.13: Wavelength dependent photocurrent spectrum of air free sample and UV treated samples.

[85] [86] corresponding to the peaks at the same positions in the absorption spectrum (inset of Fig. 3.14).

While the photocurrent from the UV-ozone treated sample shows a similar gate bias dependence (the photocurrent magnitude increases with more negative gate biases while the general shape remains unchanged), it has a significant difference. Fig. 3.14 shows the photocurrent spectra from both air free sample and UV-treated sample with the two normalized at the 668nm peak. The intensities of the four peaks in the range of 350nm to 480nm (specifically, 394 nm (3.15 eV), 420 nm (2.95 eV), 450 nm (2.76 eV) and 466 nm (2.66 eV)) are much higher in the UV-treated sample spectrum, corresponding to energy transitions larger than the HOMO-LUMO gap ($\sim$ 2 eV). We speculate that photons in this energy range form excitons [87] [88] in pentacene and enhance the charge (electron) transfer from pentacene to the -COO$^\bullet$ group introduced by the UV treatment at the surface of parylene. The neutral but electron-withdrawing -COO$^\bullet$ groups act as electron traps, dissociating the excitons and releasing free holes. This results in a larger photo response in UV-treated samples than in air-free samples at the same bias conditions.[79]

The effect of UV treatment of the dielectric surface on transport and photo response can be further elucidated by simultaneous photocurrent and transport characteristic measure-

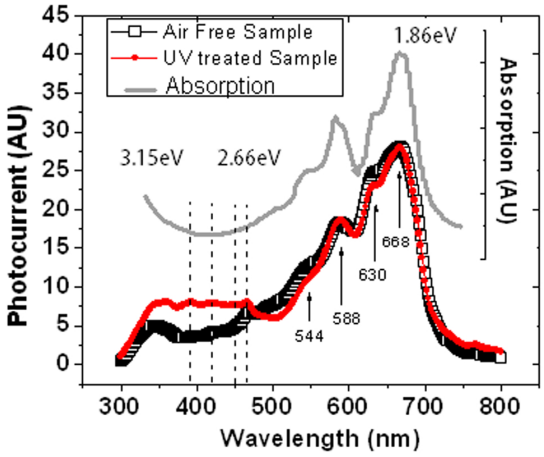

Figure 3.14: The photocurrent spectra from both air free sample and UV treated sample with the two normalized at the 668 nm peak, the inset is the absorption spectrum.

ments (I_{PC} and I_{DS} vs. V_{GS}). Several excitation wavelengths (350 nm, 400 nm, 420 nm, 465 nm, 544 nm, 588 nm, 630 nm, 668 nm) were chosen and typical data are shown in Fig. 3.15. Fig. 3.15 (a) is the gate-dependent drain current (open symbols) and photocurrent (solid symbols) from an air-free sample (squares) under $V_{DS} = -15V$ and an UV-treated sample (circles) under $V_{DS} = -10V$. Gate dependent drain current measurement shows that the threshold voltage in UV treated sample was shifted positively by 7-8 V compared to that in air-free sample. It is worth noting that the combination of oxygen and hours of light illumination can shift the threshold voltage in normal OFETs without UV treatment of the dielectric during fabrication [88]. The threshold voltage shift in our UV-treated samples is, however, mainly resulted from fixed trap charges at the interface of pentacene and UV-treated parylene, confirmed by transport measurement without illumination [89]. Although the samples here are measured in air, the chopped light illumination used is brief and weak and the effect of the measurement on the intrinsic properties of the OFETs, as measured in these devices, is minor. The photocurrent measurement also reflects the change in threshold voltage, although the exact extraction of the value from photocurrent is imprecise in the saturation region. Fig. 3.15 (b) is a similar plot for the same devices under 630 nm illumination.

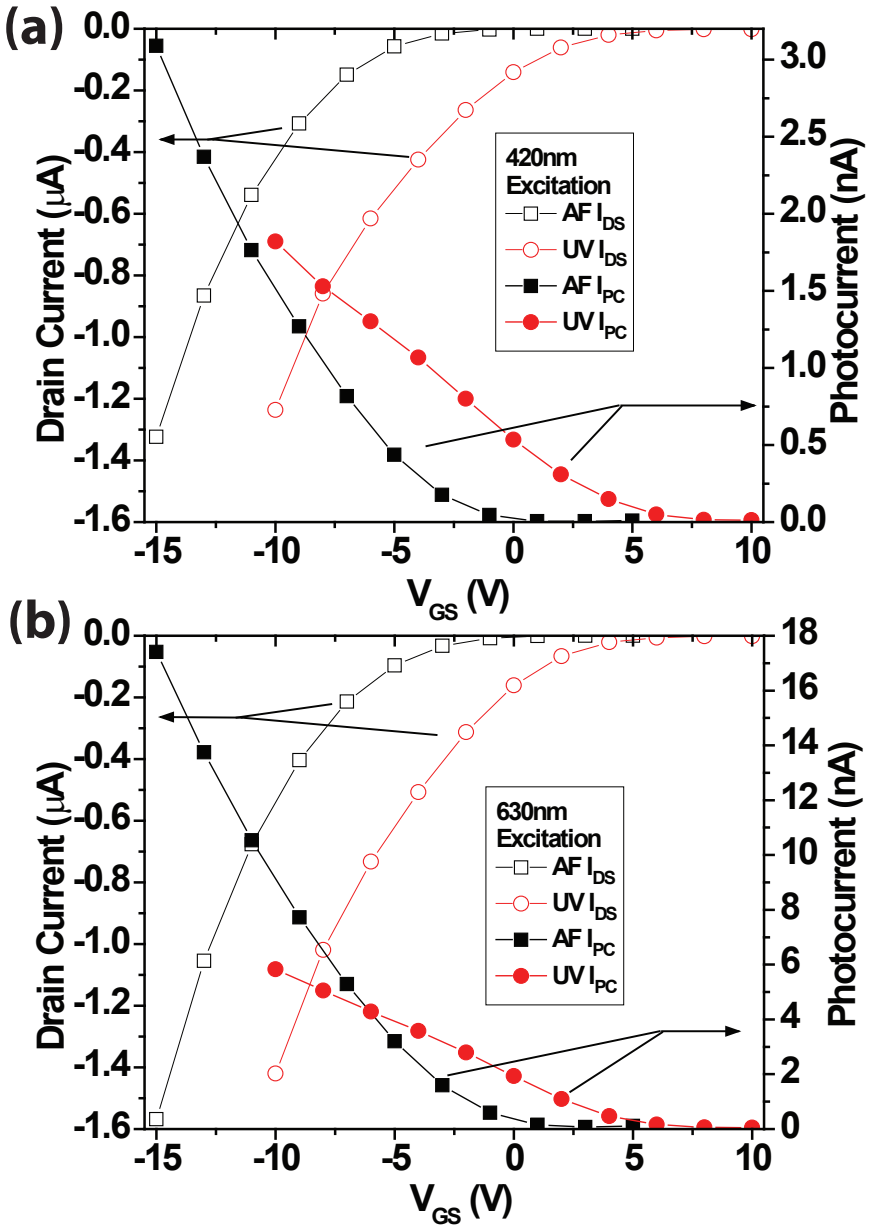

Figure 3.15: (a) the gate-dependent drain current (open symbols) and photocurrent (solid symbols) from an air-free sample (squares) under $V_{DS} = -15V$ and an UV-treated sample (circles) under $V_{DS} = -10V$. (b) similar plot as in (a) of the same devices under the same bias conditions but under 630 nm illumination.

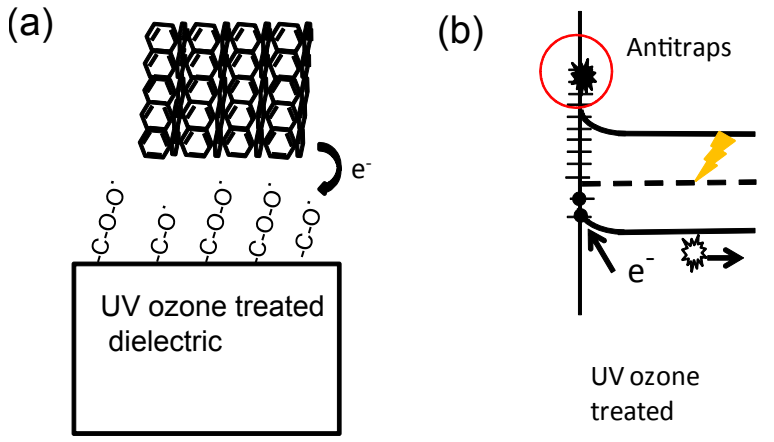

Figure 3.16: (a) shows the difference in air-free and UV-treated pentacene FETs, where the -COOH groups formed by UV treatment attract electrons from pentacene. (b) trap and release transport picture: when the device is less accumulated, and mobile carriers have to populate from the deeper states and see a higher barrier to movement. As more carriers fill the lower states, the carriers near the mobile carrier edge and are able to move with greater ease.

Fig. 3.16 shows schematically the difference between the air-free and UV-treated pentacene FETs. The UV-treated dielectric surface is partially terminated by electronegative -COO$^{\bullet}$ groups [79]. These -COO$^{\bullet}$ groups behave as acceptor-like traps and can attract electrons from pentacene. The filled traps are almost immobile and form a layer of negative charge which shifts the threshold voltage. The shift of threshold voltage can also be understood by the band bending caused by this charge transfer from pentacene to the interface. Although a fraction of the induced holes are bound by the fixed negative charges, extra holes are also freed into pentacene, confirmed by increased bulk conductivity and mobility [89].

In one possible mechanism, excitons are formed within pentacene when light is applied to the channel [87]. The unfilled -COO$^{\bullet}$ traps at the interface of pentacene and the dielectric enhance the exciton dissociation process by attracting the electrons and freeing holes which can contribute to the photocurrent. The localized states formed outside the HOMO-LUMO gap (antitraps) can also interact with the excitons by trapping the electrons and help

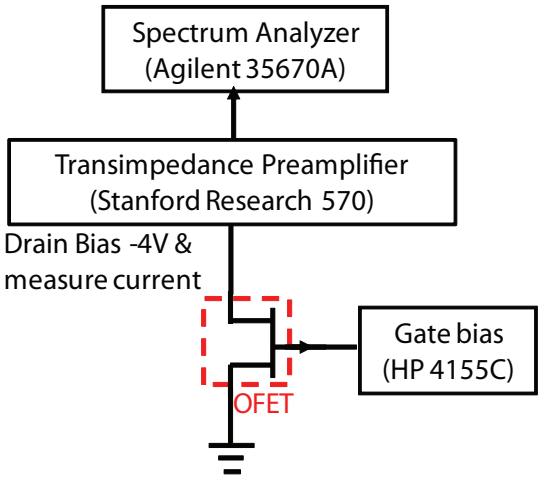

Figure 3.17: $1/f$ noise measurement configuration employed from reference [8]

dissociate the hole-electron pairs.

3.4 Probing the dielectric-semiconductor interface by $1/f$ noise

The influence of the combination centers on carrier scattering and subsequent contribution to channel noise is understood by $1/f$ noise measurement.

3.4.1 $1/f$ measurement setup

We employ the noise measurement configuration from [8] (3.17) and all the experiments are done in air. A semiconductor parameter analyzer (Agilent 4155C) provides the gate voltage and a low-noise transimpedance preamplifier (Stanford Research 570), which is battery powered, provides the drain bias and measures the drain current. The two units share a common ground which is also connected to the source contact of the device. A spectrum analyzer (Agilent 35670A) is used to record the noise power spectrum in the frequency range 1 Hz to 1.6 kHz. Each spectrum is the result of the rms averaging of 30 measurements.

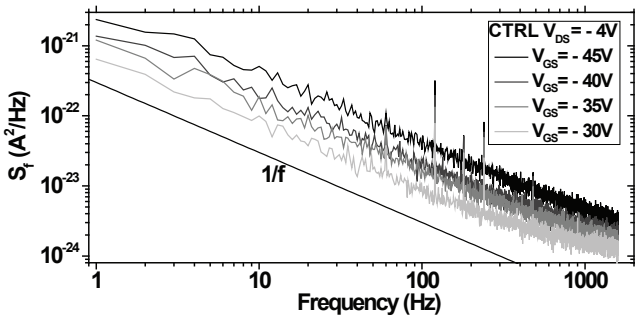

Figure 3.18: Noise power spectra for a control device show that noise power increases with more negative gate voltages or larger drain current.

3.4.2 Doping dependence of $1/f$ noise

It is generally believed that flicker noise in OFETs is generated by the hopping of carriers between trap sites. However, there is no agreement [90] [91] [92] on whether the noise generation mechanism in OFETs is caused by a carrier number fluctuation (as in the McWhorter model: trapping-detrapping of carriers in traps situated in the gate oxide, near or at the semiconductor/dielectric interface) or mobility fluctuation (as in the Hooge model: a bulk scattering phenomenon and cross section fluctuations).[93] [94] Reference [90] and [92] suggest the number fluctuation model although both believe the interaction between carriers and gate oxide is very unlikely. Despite the difference of transport and noise mechanisms in OFETs and Si MOSFETs, we take the empirical expression describing the noise power density in a transistor:[90]

$$S_f = \frac{K_F}{C_{OX} L^2} \cdot \frac{I_D^\alpha}{f^\beta} \tag{3.9}$$

where K_F is the fractional flicker noise coefficient, I_D is the drain current, L is the channel length, C_{OX} is the dielectric capacitance per unit area, and f is the frequency (in Hz). α and β are constants which relate to the energy distribution of noise-inducing states with $\alpha \sim 1 - 2$ and $\beta \sim 1 \pm 10\%$.

Fig.3.18 shows the noise power spectrum (S_f) from a control OFET as the gate bias varies. The noise increases as the gate biases becomes more negative (when the device is

more accumulated). This is also true for UV treated samples (data not shown). All the spectra follow $1/f$ trend and specifically, $\beta \sim 0.95 \pm 0.05$ for control OFETs and $\beta \sim 1.00 \pm 0.05$ for UV-treated OFETs. $|\beta|$ tends to increase slightly with more negative gate bias in all samples. In control samples under less negative gate bias, noise spectra bend up slightly in the high-frequency region since thermal noise ($\sim 4k_BT/R$, where k_B is the Boltzmann constant, T is the absolute temperature, and R is the resistance. For our devices, $4k_BT/R \sim 10^{-26} - 10^{-25}$) becomes more apparent at higher frequencies.

For convenience we define $K' = \frac{K_F}{C_{OX}L^2} \cdot I_D^{\alpha}$. By fitting the spectra with $S_f = K'/f$, K' can be extracted and plotted as a function of $I_D(V_{GS})$ for two representative UV-treated OFETs and two control OFETs (Fig.3.19(a)). There are two main differences: first, the noise level in UV-exposed devices is one order of magnitude higher than that in the control devices at the same drain current; second, the dependence of K' on drain current is different: $\alpha \sim 1.21 \pm 0.03$ and 1.14 ± 0.03 for UV 1 and UV 2 (UV-treated samples) respectively; $\alpha \sim 1.63 \pm 0.06$ and 1.56 ± 0.05 for CTRL 1 and CTRL 2 (control samples), respectively.

Reference[95] pointed out that in the linear regime, $I_D^2/K' \propto |V_{GS}|$ if noise is due to mobility fluctuations and $I_D^2/K' \propto |V_{GS}|^2$ if noise is due to number fluctuations. Fig. 3.19(b) shows that all of our samples follow $I_D^2/K' \propto |V_{GS}|$ with slopes of $(-2.07 \pm 0.06) \times 10^7$ (UV1), $(-1.59 \pm 0.04) \times 10^7$(UV2), $(-2.8 \pm 0.1) \times 10^8$ (CTRL1) and $(-1.45 \pm 0.09) \times 10^8$ (CTRL2), respectively. So there is no strong evidence of difference in noise generation mechanism between UV treated and control samples and the result implies a mobility fluctuation model. According the empirical Hooge's relation: $S_f = \frac{\alpha_H}{N} \cdot \frac{I_D^2}{f}$, where N is the total number of carriers and $N = C_{OX}WL(V_{GS} - V_{th})/e$, where W is the channel width, V_{th} is the threshold voltage, e is the charge unit of 1.6×10^{-19}C and α_H is the Hooge's parameter. Comparing this work $S_f = K'/f$, we have $\alpha_H = \frac{N}{I_D^2/K'}$. Based Fig.3.19(b), the Hooge's parameter α_H for UV treated samples is around 1 - 3 and α_H for control samples is around 0.1 - 0.3.

UV-ozone forms electron accepting sites at the surface of dielectric,[96] [79] which extract electrons from pentacene and induce holes in pentacene.[7] [97] The trapped electrons form a layer of fixed negative charges, which shifts the threshold voltage.[89] These fixed charges further appear to serve as scattering sites for induced and accumulated holes, leading to a higher noise level.

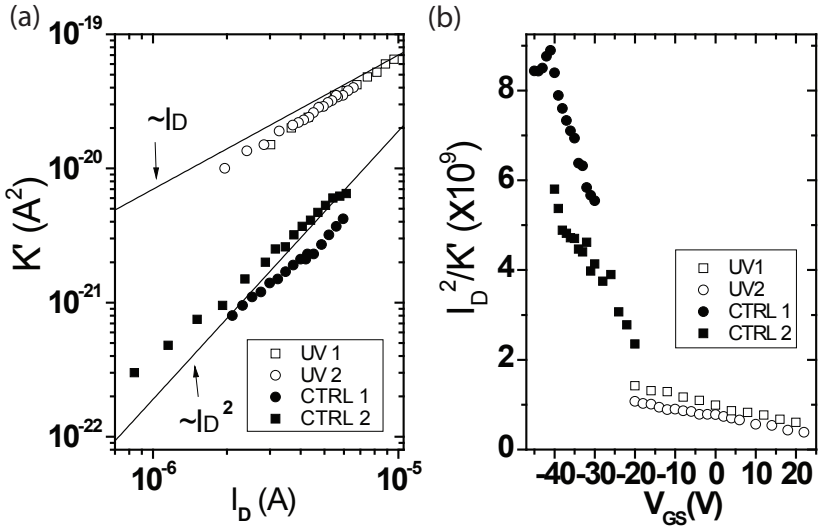

Figure 3.19: (a)The plot of K' as a function of varied drain current (I_D, as a result of varied gate bias V_{GS}) for two UV-exposed devices and two control devices. The lines are guidelines of I_D^2 and I_D dependence. Please refer to text for the exact fitting slopes. (b)The plot of I_D^2/K' as a function of V_{GS} for the same devices. The linear dependence indicates a mobility fluctuation model.

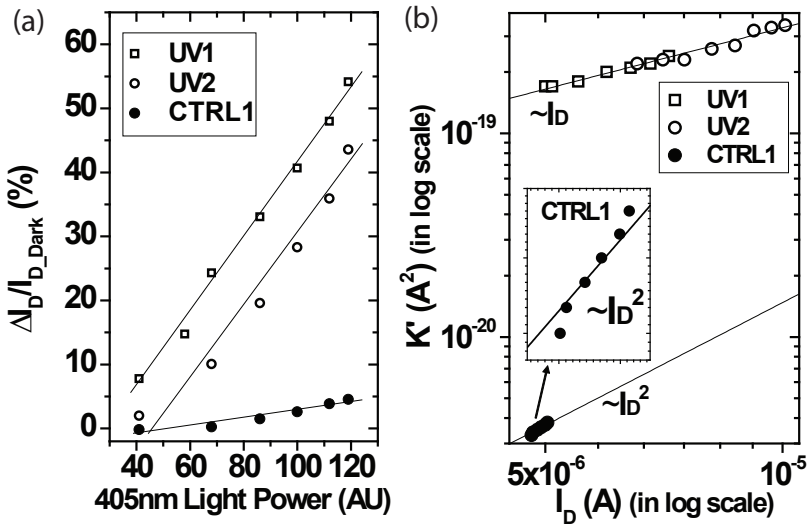

Figure 3.20: (a)Drain current change under 405nm LED illumination as a function of illumination power. The drain current change is calculated as $\Delta I_D/I_{D\_Dark} = (I_D - I_{D\_Dark})/I_{D\_Dark}$. The control sample (solid dots) is under $V_{GS} = -40V$ and $V_{DS} = -4V$. The UV treated samples (open squares and spheres) are under $V_{GS} = 0V$ and $V_{DS} = -4V$. (b)The plot of K' for control and UV OFETs as a function of varied I_D resulted from illumination. Inset is the zoomed plot of control sample data. The lines in all plots are guidelines of I_D^2 and I_D dependence. Please refer to text for the exact fitting slopes.

One possible explanation for the power-law dependence of the UV-treated devices is that a constant number of scattering sites is responsible for the noise, and as a consequence the noise increases nearly linearly with the available density of carriers to scatter ($\alpha = 1.1$). The control device, by contrast, is able to access a different density of traps as the Fermi level moves with increasing gate bias, allowing an increasing density of accessible scattering states together with an increased number of carriers. This gives a superlinear response in the noise characteristic ($\alpha = 1.6$). The ability of states outside the HOMO-LUMO gap to influence transport is a characteristic of disordered semiconductors; carriers are localized and are not thermalized to the frontier gap energies.[97]

3.4.3 Illumination dependence of *1/f* noise

Photocurrent excitation was also studied as an approach to inject charge into the samples. Photocurrent excitation allows the introduction of charge without changing the Fermi level, permitting probing of the noise characteristic without changing the applied bias. It has been shown that 405nm illumination selectively excites carriers from interfacial states at the interface of pentacene and gate dielectric, and is absorbed weakly by pentacene due to its low absorption cross-section above the HOMO-LUMO gap.[97] [88] The OFET channel was illuminated by 405 nm light from a regulated LED, and the drain current before (I_{D_Dark}) and during (I_D) was measured and plotted as $\Delta I_D/I_{D\_Dark} = (I_D - I_{D\_Dark})/I_{D\_Dark}$ (Fig.3.20(a)). The control sample was under $V_{GS} = -40V$ and $V_{DS} = -4V$. The UV-exposed sample is under $V_{GS} = 0V$ and $V_{DS} = -4V$. In the UV-treated OFETs, the illumination excited more carriers than the control device and led to a greater photocurrent magnitude.

The $1/f$ noise spectrum for the UV-treated device follows $K' \sim I_d^\alpha$ with $\alpha \sim 0.96 \pm 0.05$ for UV 1 and 1.1 ± 0.1 for UV 2, respectively (Fig.3.20(b)). The noise level is generally higher than that without light exposure (Fig.3.19). For the control device, the noise level is comparable to that in Fig.3.19 but with an $\alpha \sim 2.8 \pm 0.2$. When 405 nm light is applied to the channel, photons (3.1 eV) appear to transfer excess energy to excited pentacene molecules, making the electron transfer more effective from pentacene to -O- and -O-O- bonds at the dielectric surface, which is treated by UV ozone and generating holes into the channel. [7][97][88] We observe the noise level from these photogenerated carriers is higher than that from the gate-accumulated carriers. The significant increase in the slope of the noise characteristic in the control device is possibly caused by the photoexcitation of carriers from filled states, leading to an increase in available scattering sites. Further investigation of this effect is underway.

3.5 Conclusion

The dipole interaction and recombination interaction with charges have been discussed in this chapter. The UV ozone treatment of the dielectric and its effect on electrical perfor-

mance have been studied by spectral photocurrent and $1/f$ noise measurement.

The wavelength resolved photocurrent spectrum demonstrates that photons with energies larger than the pentacene HOMO-LUMO gap form excitons which more efficiently dissociate into electrons and holes thanks to the -COOH group introduced by UV-ozone treatment of the dielectric layer before deposition of the semiconductor. These electron acceptor-like traps are responsible for the positive shift in threshold voltage seen in UV-treated samples.

We have examined the influence of gate dielectric surface groups introduced by UV-ozone treatment on the $1/f$ noise characteristics of OFETs. Devices with a UV-ozone treated gate dielectric were compared to otherwise identical control devices fabricated without an air break. Noise power in the control devices is one order of magnitude lower than that in UV-treated OFETs, and proportional to $I_D^{1.6}$. Noise in the UV-treated samples is proportional to $I_D^{1.1}$. We attribute the main noise source in the UV OFETs to acceptor-like traps at the interface of the semiconductor and dielectric introduced by UV treatment of the dielectric. We also confirmed that the same noise spectrum, and therefore mechanism, holds for photogenerated charges the UV treated samples. An increased noise slope is observed in the photogenerated charges in the control samples, possibly because of an interaction with available trap states in those devices.

Chapter 4

Improving the Semiconductor-Contact Interface by Thiol Treatment

One approach developed to improve the performance of bottom contact source/drain electrodes is to treat the contacts with thiols before deposition of the semiconductor. There is evidence indicating that improvement is due to both morphological effects and improved work function matching. Especially suggestive evidence shows that thiols that increase the effective work function of the contacts (*e.g.* fluorinated thiols) yield better device performance than work function decreasing thiols (*e.g.* alkane thiols). The effect of thiol treatment on semiconductor morphology is first reviewed in this chapter. Energy barrier is taken into consideration of the difference between different thiols which have similar morphology effects. We compare two technologically relevant thiol treatments, an alkane thiol (1-hexadecanethiol), and a fluorinated thiol (pentafluorobenzenethiol), in pentacene organic field effect transistors. Using *in-situ* semiconductor deposition, X-ray photoemission, and X-ray absorption spectroscopy, we were able to directly observe the interaction between the semiconductor and the thiol-treated gold layers. Our spectroscopic analysis suggests that there is not a site-specific chemical reaction between the pentacene and the thiol molecules. A homogeneous standing-up pentacene orientation was observed in both treated substrates,

consistent with the morphological improvement expected from thiol treatment in both samples. Our study shows that both the HOMO-Fermi level offset and C 1s binding energy are shifted in the two thiol systems, which can be explained by varied dipole direction within the two thiols, causing a change in surface potential. The additional improvement of the electrical performance in the pentafluorobenzenethiol case is originated by a reduced hole injection barrier that is also associated with an increase of the density of states in the LUMO.

4.1 Effect of thiol treatment on morphology

Many printing and lithographic OFET processes pattern the source and drain contacts before the semiconductor is deposited.[98] This bottom contact approach allows processing of the contacts without exposing the semiconductor to process chemicals, which is often detrimental to semiconductor performance. Bottom contact geometries, however, typically have decreased performance when compared with top contact devices (Fig. 4.1 (a)), exhibiting both increased contact resistance and reduced channel mobilities. In some cases, this is due to a morphological mismatch in the semiconductor between the contact and the channel [99] and possibly a barrier to carrier injection at the metal-semiconductor interface.[100] [101] A number of structural studies have confirmed the ability to engineer the morphology of organic semiconductors deposited on metals via thiol treatment in small molecule [101] (see Fig. 4.1(b)) and polymer semiconductors.[102] These surface treatment on the source and drain metal of OFETs have demonstrated improvements to the contact resistance and channel transistor performance.[100] [103]

4.2 The techniques to measure molecular energy levels

4.2.1 Ultraviolet photoelectron spectroscopy (UPS) and X-ray photoelectron spectroscopy (XPS)

Both UPS and XPS are photoemission spectroscopy, where the sample surface is irradiated by mono-energetic photons and the emitted electrons are detected by an electron energy

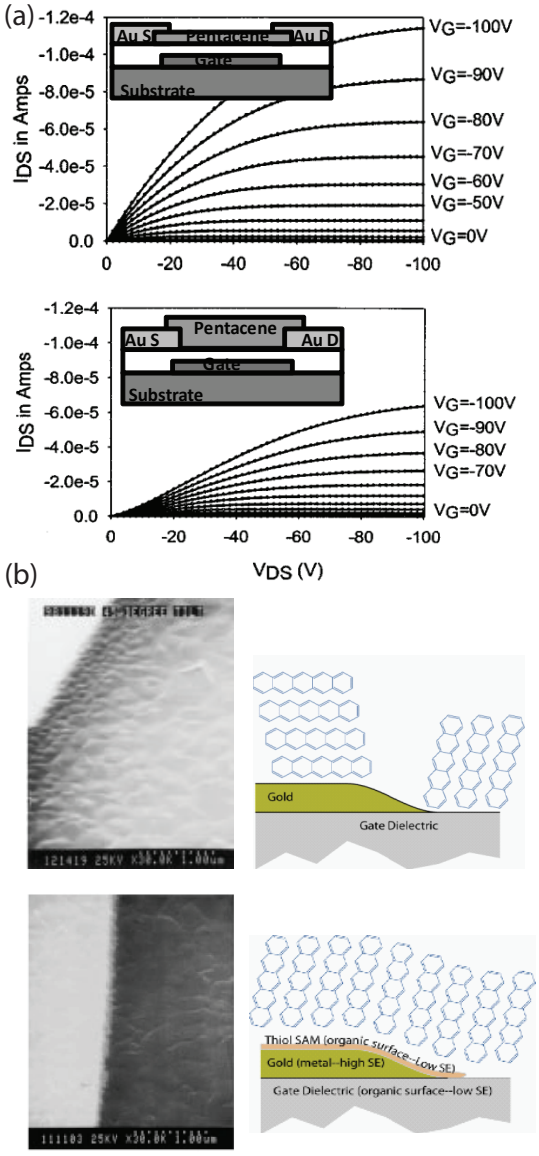

Figure 4.1: Effect of thiol treatment on pentacene morphology. (a)bottom-contact structure has worse performance than top-contact structure. (b)pentacene forms different microstructures on different surfaces: they tend to lie down on the high-energy metal surface and stand up on the low-energy dielectric surface. This mismatch in microstructure deteriorates the electrical performance. By depositing a self-assembled monolayer of thiol on Au surface, the pentacene forms continuous structure across the channel and the electrical performance is recovered.

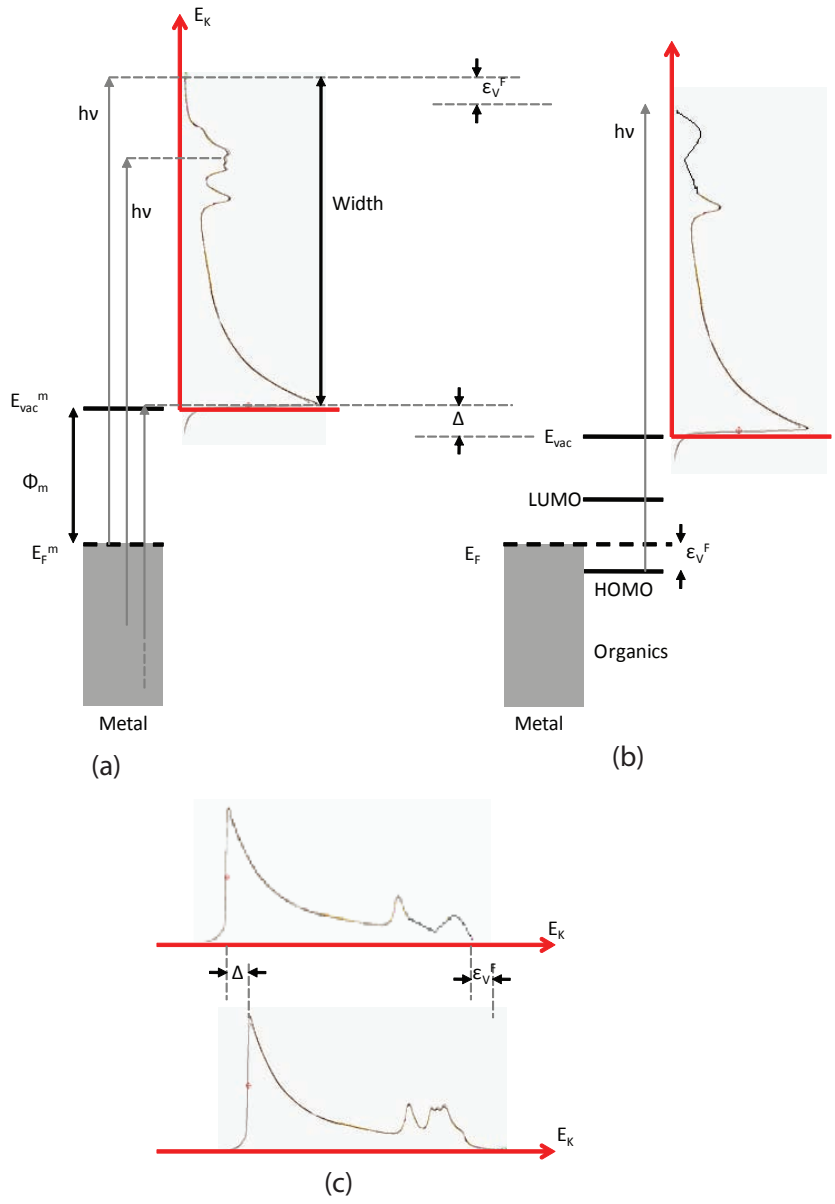

Figure 4.2: Principle of UPS adapted from [9]. (a) is the UPS measurement to determine the work function of a metal surface. It also includes the Au UPS spectrum as an example. (b) shows the UPS from the organic layer deposited on the metal surface. It also indicates how the vacuum level shifts as the organic layer is deposited on the metal. (c) stacks the two measurements with alignment at the Fermi edge.

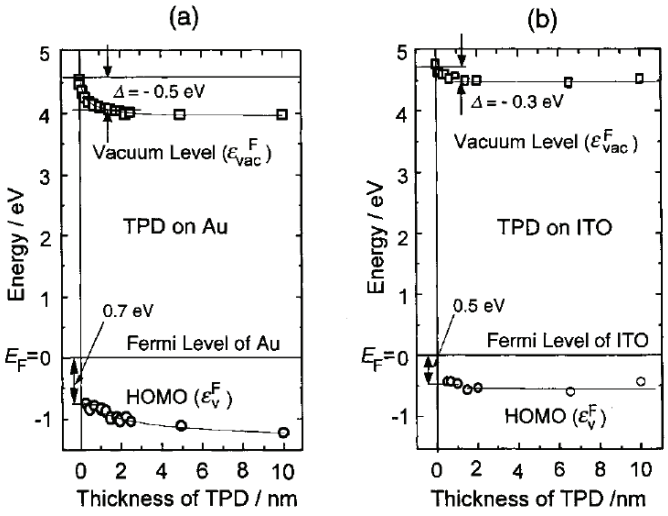

Figure 4.3: The thickness dependence of the values of Δ (vacuum level shift) and HOMO edge shift for TPD on Au and ITO surfaces taken from reference [9].

spectrometer. The energy of photons in XPS can vary from 100 eV to 1000 eV, while the UPS uses He I discharge of $h\nu = 21.2$ eV. High energy XPS is usually used to detect core electrons such as $1s$, $2s$ and $2p$ electrons; low energy XPS and UPS are usually used to measure the HOMO bands or valence bands of materials. Both of these techniques are surface probes. Although the excitation photons can penetrate 1-10 μ m down into the surface, the electrons being detected are from several nanometers within the sample surface.

The principle of UPS is shown in Fig. 4.2, which is adapted from reference [9]. (a) is the UPS measurement to determine the work function of a metal surface. It also includes the Au UPS spectrum as an example. Electrons are kicked out from the valence bands of a metal by the photons with energy of 21.2 eV. The electrons with largest kinetic energy are the ones from Fermi edge; the electrons with lowest kinetic energy are the ones with just enough energies to escape from the surface. Further from the Fermi edge, the density of states increases and this is why the spectrum intensity increases tremendously, until it drops dramatically because the electrons further down in valence bands can no longer escape the surface. So the work function of the metal, defined by the difference from Fermi energy to

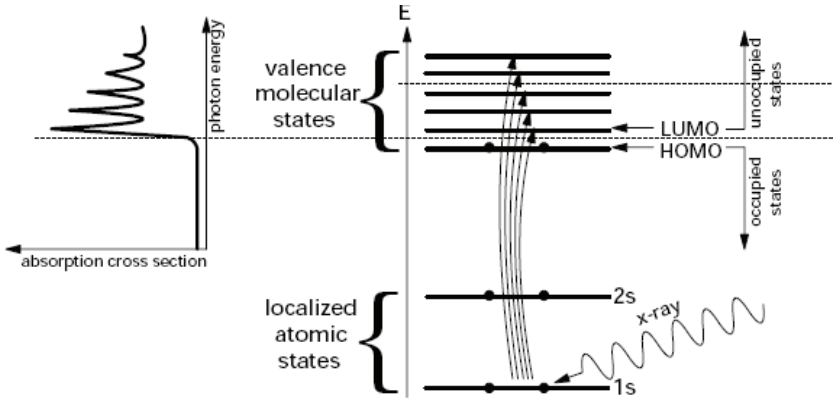

Figure 4.4: The principle of NEXAFS taken from reference.[10]

the vacuum level, can be determined as:

$$\Phi_m = h\nu - Width \tag{4.1}$$

$Width$ is the width of the spectrum of electron kinetic energy, from Fermi edge to the sharp drop edge. (b) shows the UPS from the organic layer deposited on the metal surface. (b) also shows how to measure vacuum level shifts as the organic layer is deposited on the metal. As an example, the thickness dependence of the values of Δ (vacuum level shift) and HOMO edge shift is shown in Fig. 4.3 for N,N'-diphenyl-N,N'-(3-methylphenyl)-1,1'-biphenyl-4,4'diamine (TPD). The plots clearly depicts the energy alignment at the interface of organic semiconductor and metal. There is no alignment issue for a UPS measurement since all the spectra are taken with Fermi level grounded and the incident photon energy is fixed. However, this is not the case for XPS measurement where the photon energy can vary over time. So it is advisable that the XPS peaks of the metal are taken as reference to align the spectra.

4.2.2 Near-edge x-ray absorption fine structure (NEXAFS)

NEXAFS is a photon-absorption technique to measure unoccupied states in molecular orbitals. Its operation principle is shown in Fig. 4.4. The electrons from $1s$ core levels are

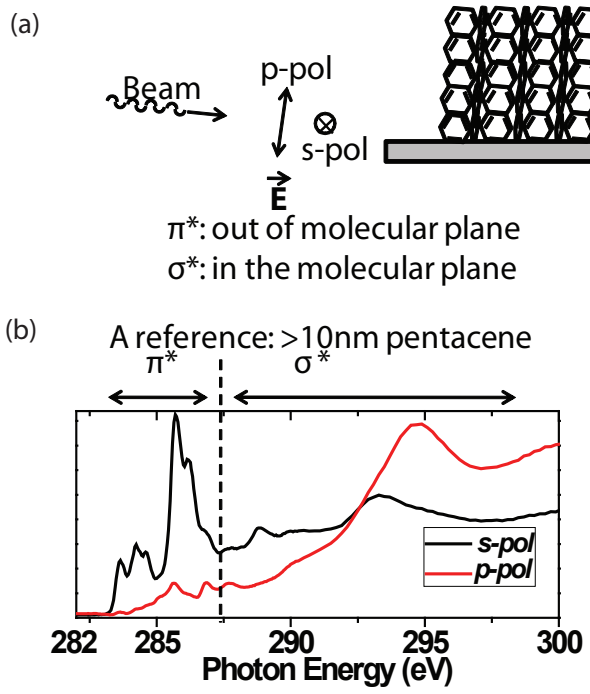

Figure 4.5: the thickness dependence of the values of Δ (vacuum level shift) and HOMO edge shift for TPD on Au and ITO surfaces.

excited to one of the unfilled molecular states, followed by the de-excitation through fluorescence or Auger electrons. When the energy of the excited electrons match that of an empty state, the absorption gets strengthened and a peak is shown in NEXAFS spectrum. Since the absorption depends on the initial core atomic levels and the unoccupied molecular states, the spectrum shows the information of both the atomic chemical environment and the molecular empty states. By sweeping the excitation energy, NEXAFS effectively maps the unfilled moleular states (LUMOs).

NEXAFS is also a sensitive method to determine molecular orientation and thus gives important information about material microstructure. As shown in Fig. 4.5, on a low energy surface, pentacene tends to stand up and closely pack on the surface. In such a configuration, π^* states can only be excited by s polarization. σ^* states can be excited by both polarizations and p polarization should give stronger resonance. So by changing the incident beam polarizations one should see the π^* bond intensity change when changing the polarization. This is what we see in the thick pentacene film as a reference. The

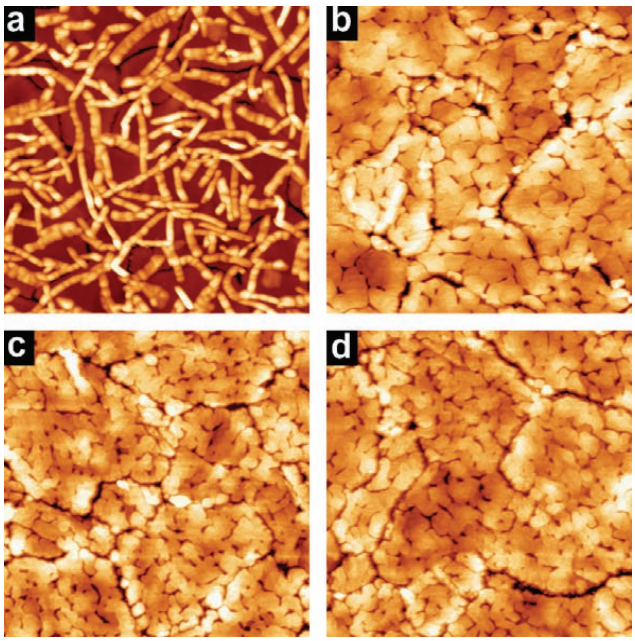

Figure 4.6: AFM images from reference [11](intermittent contact, scan size: 5 by 5 μm^2) of 8 nm-thick pentacene films deposited on polycrystalline gold substrates for various surface treatments. (a) Bare gold (z-scale: 100 nm); (b) gold with DT SAM (z-scale: 35 nm); (c) gold with PFDT SAM (z-scale: 35 nm); (d) gold with PHDT SAM (z-scale: 40 nm).

thick pentacene film is taken as a reference because of its known polycrystalline thin-film structure with molecules standing up on the surface.

4.3 Fluorinated versus alkane thiols

While different thiols tend to have similar morphological effect on the subsequent semiconductor growth (Fig. 4.6(a)), they have different electrical impact(Fig. 4.6(b)). In particular, there has been significant work in developing fluorinated thiol treatments for p-type organic semiconductors,[12] which effectively increase the work function of the contact layer by creating a dipole layer on the gold. It has been hypothesized that such an interface further decreases the barrier between the semiconductor and the contact, leading to improved access between the contact and highest occupied molecular orbital (HOMO) of the

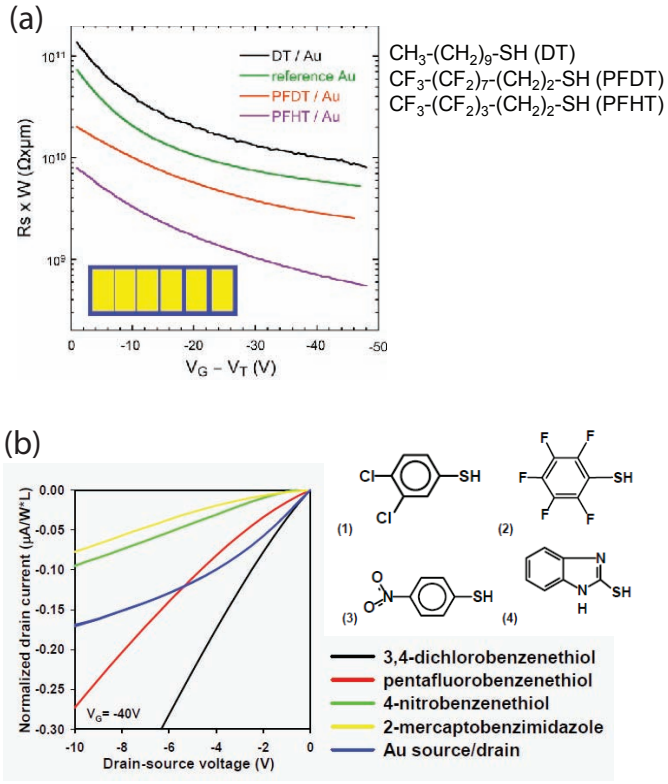

Figure 4.7: (a)Gate bias dependent contact resistance extracted from OFETs samples with contacts under different thiol treatment from reference [11]. (b)drain current vs. drain voltage from OFETs samples with contacts under different thiol treatment from reference[12].

semiconductor. The direct consequent creation of free charge due to the charge withdrawal reaction is also proposed as a reason.[104] Ultraviolet photoelectron spectroscopy (UPS) measurements have been performed on a range of SAMs to observe the effective change in the work function [105] [106] and led much of the work determining the suitability of these layers to improve organic semiconductor devices.[100] [11]

In this work, using *in-situ* semiconductor deposition together with x-ray photoelectron spectroscopy (XPS) and near-edge x-ray absorption fine structure (NEXAFS), we are able to directly observe the interaction in two technologically relevant organic field effect transistor device stacks. This work directly measures the interaction between pentacene and the two thiols which have been applied to contact improvement in pentacene-based OFETs: an alkane thiol (1-hexadecanethiol) [101] and a fluorinated thiol (pentafluorobenzenethiol).[107]

4.3.1 Experiment setups at Aloisa beamline

The two thiol SAMs solutions were prepared with 1% thiol in ethanol. Glass was coated with 5 nm of Cr for adhesion and 50 nm of Au using thermal evaporation. The samples were submerged in the thiol solutions immediately after evaporation to avoid contamination. The experimental samples were mounted on a sample holder with a cold finger for cooling and filaments for heating. Pentacene was evaporated *in-situ* in ultra-high vacuum from a boron nitride Knudsen cell (at ∼500 K), while keeping the substrate at room temperature, at a constant rate of 1 Å/min as monitored by a calibrated quartz microbalance. The thickness of single layer pentacene was calibrated *ex-situ* using AFM. In order to prevent radiation damage, we only irradiated the sample with the X-ray beam while the sample temperature was below 210K. As a check on the integrity of the sample, we periodically monitored the sulfur $2p$ core level, where thiol decomposition on gold would be witnessed by the appearance of a component at a binding energy 1 eV lower than the characteristic gold-thiolate spectral line at B.E. = 162 eV. [108; 109] Thanks to the sample cooling and the spread of the beam over the surface due to the grazing incidence, the thiol structure remained unaltered throughout the measurements.

Measurements were taken at the ALOISA beamline at the Elettra Synchrotron in Trieste, Italy. Fig. 4.8 shows the two chamber structure of Aloisa - one is for thin film

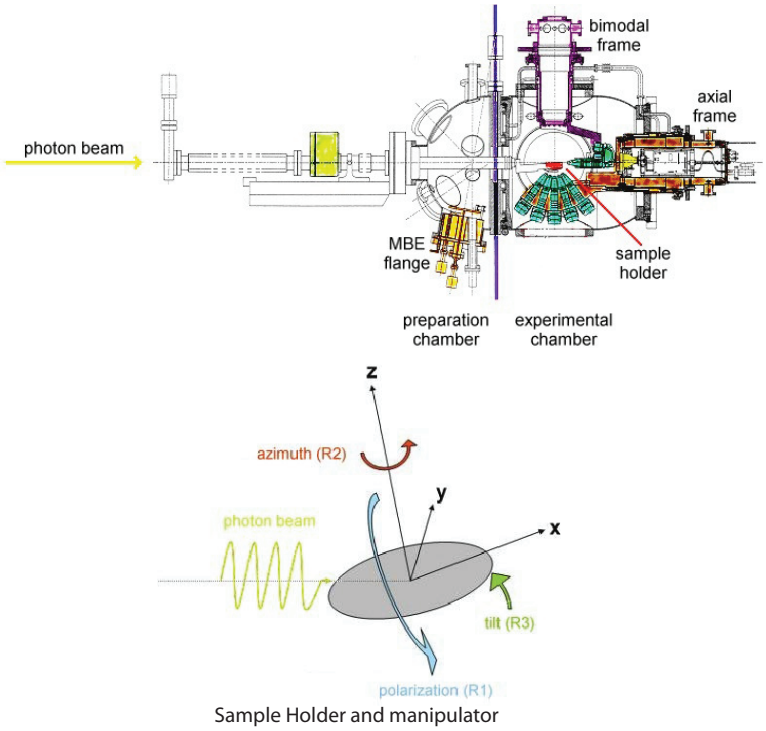

Figure 4.8: Figure taken from reference [10]. Aloisa consists of two chambers: one is for thin film deposition and the other spectroscopic analysis. The sample holder has six-degree freedom of manipulation. The beam incidents from a grazing angle.

deposition and the other spectroscopic analysis. Core level XPS was measured at photon energy of 450, 650, 760 eV (photon energy resolution estimated at 150, 250 and 350 meV, respectively), while valence band spectra were taken at 130 eV. Core level photoemission spectra have been aligned against the binding energy of the Au 4f peaks.[110] All spectra were taken at a grazing incidence $\alpha = 4°$ and close to normal emission ($90° - \alpha$) with an angularly resolved (FWHM $\sim 3°$) spectrometer. The overall energy resolution for valence band spectra was set to 0.15 eV. NEXAFS spectra were collected at the C K-edge by means of a channeltron provided with a retarding grid set to -230 V. The x-ray absorption measurements were taken at a constant grazing incidence $\alpha = 6°$, in Transverse Magnetic and Transverse Electric polarization (p and s polarization, respectively) by rotating the sample surface around the photon beam axis. Absolute calibration of the photon energy has been obtained a posteriori using the fingerprint of carbon contamination in the drain current measured on the gold coating of the last beamline mirror. The corresponding spectral line was previously calibrated by real time acquisition of gas phase x-ray absorption spectroscopy (XAS) from CO and the drain current.[111]

4.3.2 HOMO comparison by the XPS

HOMO states of pentacene deposited on the thiol/Au stack are measured using XPS at a photon energy of 130 eV. Fig 4.9(a) shows the XPS spectrum for 1-hexadecanethiol (Hex-thiol) on gold (grey line) and the XPS spectrum of a single layer (SL) of pentacene deposited *in-situ* on the 1-hexadecanethiol/gold surface (black line). Likewise, Fig 4.9(b) shows the XPS spectra for the pentafluorobenzenethiol (PFB) on gold, both with (black) and without (grey) SL pentacene. For the pentacene deposited on hexadecanethiol (Fig 4.9(a)), the HOMO peak is centered at B.E. = 1.1 eV with a FWHM of 0.7 eV. This is consistent with the spectra of SL pentacene grown on silicon dioxide [112] and bulk pentacene (50 nm) grown on gold.[113] The spectrum of the pentacene grown on the pentafluorobenzenethiol (Fig 4.9(b)) shows a peak centered at B.E. = 0.6 eV with a FWHM around 0.6 eV. Accordingly, the HOMO edge (as determined by linear extrapolation of the low binding energy onset) shifts from a binding energy of 0.5 eV in pentacene/Hex-thiol/Au sample to B.E. $\leq$ 0.1 eV in pentacene/PFB/Au sample. In the latter case, the decreased hole injection barrier from

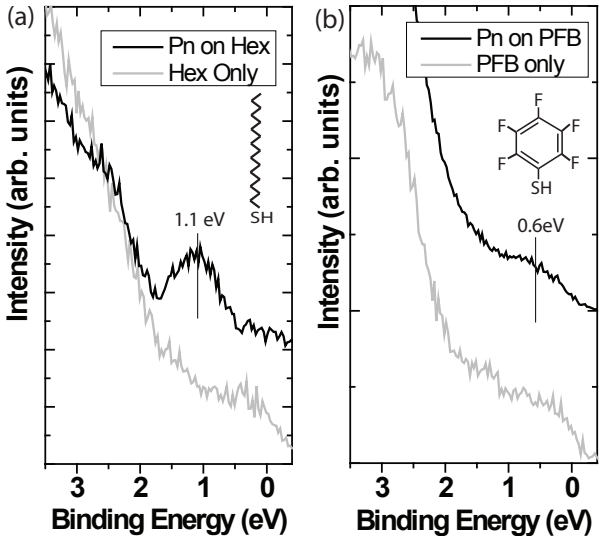

Figure 4.9: The valence band edge measured on the hexadecanethiol (Hex-thiol) (a) and pentafluorobenzenethiol (PFB) (b) treated samples. The HOMO edge shifts from 0.5 eV in pentacene/Hex-thiol/Au sample to 0.1 eV in pentacene/PFB/Au sample, showing decreased hole injection barrier from Au contact to pentacene in the latter case which leads to an improved contact between the semiconductor and the source/drain.

Au contact to pentacene leads to an improved contact between the semiconductor and the source/drain.

4.3.3 C 1*s* core electrons

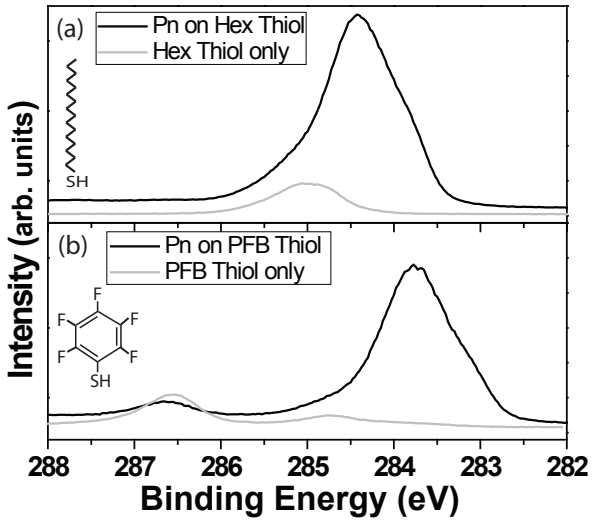

Figure 4.10: X-ray photoelectron spectroscopy (XPS) taken exciting the 1*s* carbon orbital on the hexadecanethiol (a) and pentafluorobenzenethiol (b) samples. The shape of peaks in both samples resembles the shape of peaks in gas-phase and thin-film-phase pentacene formed on non-dipole interface. The shift of the C 1*s* peaks in pentacene/PFB/Au to the lower B.E. is caused by the dipole in the pentacene/PFB/Au.

The characteristics of interaction between pentacene and the two thiols can be further analyzed by looking at the respective carbon 1*s* core levels. The C 1*s* XPS spectra, shown in Fig. 4.10, are taken at a photon energy of 450 eV. The grey lines are from thiols on gold before depositing pentacene and the black lines are the spectra after depositing SL pentacene *in-situ*. Again, the spectra are aligned against the bulk component of the Au 4f doublet at 84eV.[110] The C 1*s* peak for pentacene/Hex-thiol/Au shows an asymmetric shape with two peaks centered at 284.4 eV and 283.8 eV with a FWHM of 0.6 eV and 0.4 eV, respectively. This shape resembles the spectrum of gas-phase pentacene [114] and a monolayer of pentacene on benzenethiol/Cu,[115] which is expected to have same standing-up thin film structure as the pentacene in this experiment. Except for a slight broadening

(0.1 eV) and a rigid shift of 0.6 eV to the lower B.E. for both peaks, the C 1s spectrum of pentacene/PFB/Au is the same in shape as that of pentacene/Hex-thiol/Au.

As we later discuss, upon the deposition of a SL pentacene, there may be some charge exchange between pentacene and thiol molecules to align the Fermi energies. However, the similar shape of C 1s implies that the electrons withdrawn from or given to pentacene are not preferentially sitting at any of the six nonequivalent carbon atoms in pentacene. We believe the charge exchange occurs only at the shallow HOMO states, where the π electrons are delocalized along the molecule of the pentacene, leaving the core carbon electrons unaffected. Typically, site-specific changes in the core electrons caused by pentacene orientation or changes of the local electronic environment (such as in chemical reaction) appear as either energy or intensity shifts in these two carbon peaks.[115] [116] The shape of C 1s peaks for pentacene/Hex-thiol/Au and pentacene/PFB-thiol/Au resemble those of thin-film-phase pentacene formed on a non-dipolar interface,[116] where there is negligible electronic interaction between pentacene and the thiol surface. As we later indicate, the rigid 0.6 eV shift of the C 1s peaks in pentacene/PFB/Au is due to the molecule dipoles with different directions and moments within the two thiols.

4.3.4 LUMO comparison by NEXAFS

Fig 4.11 showing the C K-edge NEXAFS spectra offers verification of the pentacene structure and further evidence of the charge interaction between pentacene and the pentafluorobenzenethiol. For the spectra taken in s-pol, resonance peaks in the lower-energy region (283 eV - 288 eV) are assigned to the excitations from C 1s core level to the empty π^* orbitals corresponding to the LUMO (283-285 eV) and LUMO+1 (285-288 eV) transition. The broader features in the high-energy region (292 eV - 310 eV) are due to excitations of σ^* orbitals.[114] [111] [115] [117] The resonance peak at 288.8 eV between the above two regions, absent in the gas-phase spectrum,[114] is attributed to molecule-molecule interaction in the deposited pentacene layers.[115] [111] Residual contributions from the substrates can be also detected. In particular, the small peak at 287.8 eV in Fig. Fig 4.11 (a) stems from the main transition line of PFB (Fig 4.11 (d)). The broader spectrum taken on the HEX substrate additionally affects the LUMO+1 group and the valley at 285 eV between the

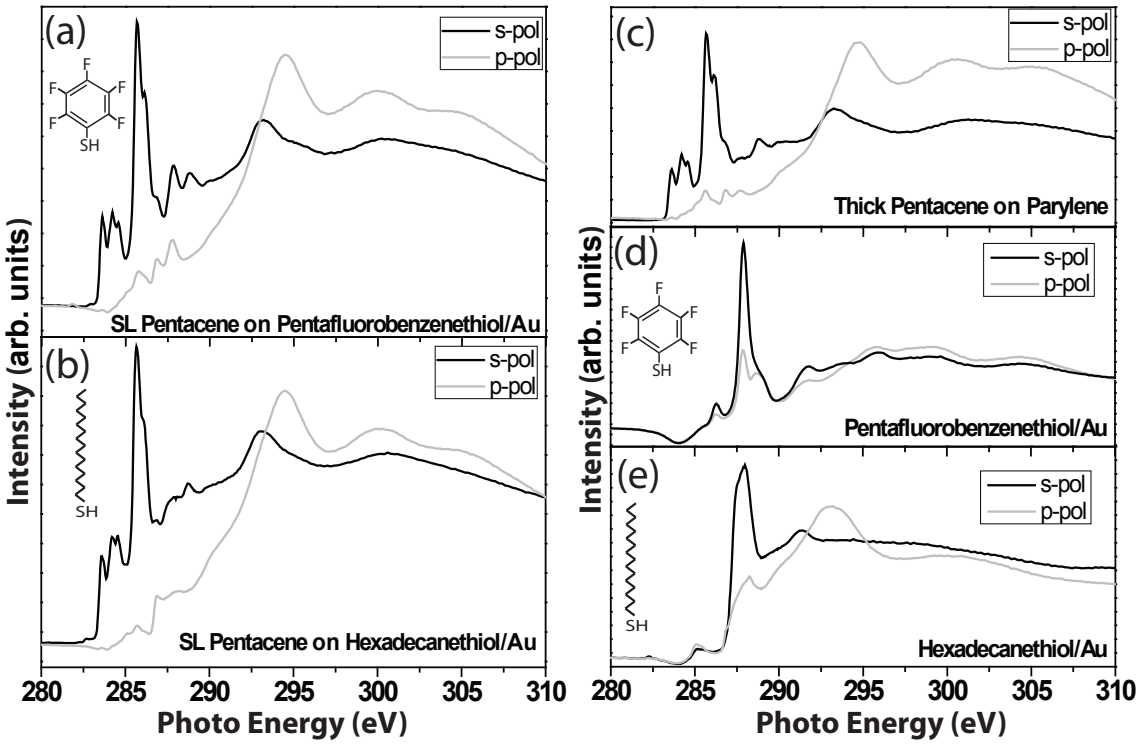

Figure 4.11: NEXAFS taken on the pentafluorobenzenethiol with a monolayer of pentacene (a), hexadecanethiol with a monolayer of pentacene (b), thick pentacene (>10nm) on parylene (c), pentafluorobenzenethiol only on Au (d) and hexadecanethiol only on Au (e).

LUMO and LUMO+1. The intensity difference in π^* region between the s-pol and p-pol absorption spectra indicates the formation of a well-ordered layer of pentacene, with the pentacene molecules preferentially standing up in all samples.[111] [115] Similar morphology of pentacene on varied thiols is confirmed by AFM in this study (data not shown) and other studies.[11] This standing-up morphology is important in the operation of pentacene based OFETs.

As a reference, the NEXAFS spectrum of thick (>10 nm) pentacene on a parylene/Au substrate is shown in Fig 4.11(c). The intensity weight of the π^* components for pentacene SL on hexadecanethiol (Fig 4.11(b)) and the thick pentacene film (Fig 4.11(c)) are comparable to each other. This confirms that there is a negligible charge exchange between the pentacene SL and the hexadecanethiol. However, when pentacene is deposited on the pentafluorobenzenethiol, electron density is transferred from the pentacene band edge (primarily the HOMO shallow states) to the thiol molecules to align the Fermi energies. Electrons then redistribute among the LUMO and HOMO states making available new empty states at the LUMO edge.[9] In Fig 4.12, it is clearly seen that the NEXAFS intensity of the first fine structure in the LUMO is enhanced for pentacene grown on pentafluorobenzenethiol. The intensity weight of the first LUMO state also appears larger than in the bulk and than in the gas phase. Because of the atomic-like origin of these fine structures,[114] their relative weight should remain unaltered in the absence of a major rehybridization or of a direct interaction with the substrate of the corresponding atoms. A direct interaction is also excluded since the first LUMO state stems from the six carbon rim-atoms close to the center of the standing-up pentacene.[114] The charge retraction from pentacene is effectively pushing a new state above the Fermi level that overlaps the existing LUMO, as evidenced by the LUMO fitting analysis of Fig 4.12. For comparison, the reverse mechanism is also observed when injecting electrons into thin organic films by alkali doping; as the LUMO gradually disappears due to charge filling a new state (HOMO) appears below the Fermi level that gradually shifts to lower binding energy as the charge injection increases.[118] [119]

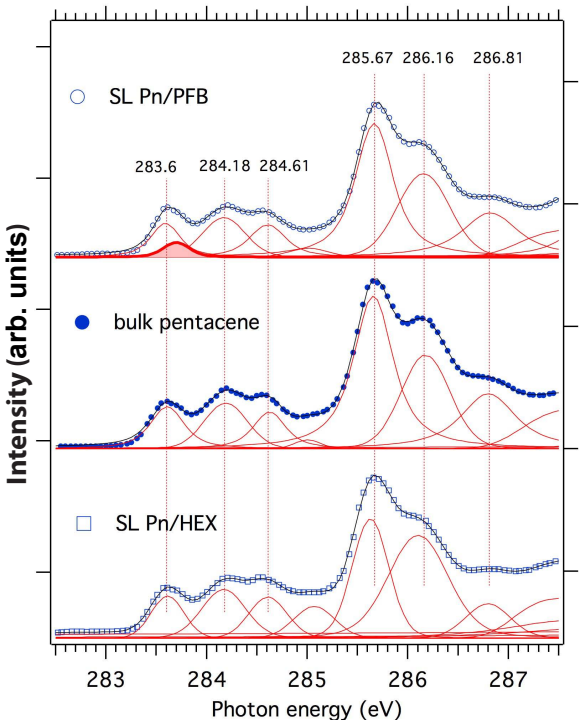

Figure 4.12: Detailed comparison of the Pn/PFB and PN/HEX LUMO states (open markers in the top and bottom panels, respectively) with the pentacene bulk states from the thick film (filled markers in the middle panel). Multiple component fitting lines are superimposed on the experimental data points. We first fitted the thick film to Voigt functions (full lines) with free fitting parameters. Then, the NEXAFS spectrum of the Pn/PFB SL was fitted by constraining the LUMO and LUMO+1 states to have the same energy position and shape parameters of the corresponding peaks in the thick film (i.e. only the peak intensity was left as fitting parameter). In the Pn/PFB spectrum, an additional peak (shadowed) accounts for the increase of the density of states at the NEXAFS edge. The fitting constraints were relaxed for the Pn/HEX spectrum in the 285-288 eV range because of the substrate contribution to the NEXAFS spectrum.

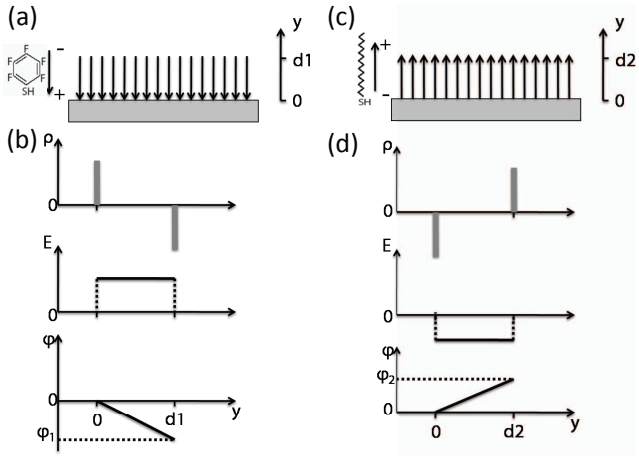

Figure 4.13: A schematic of dipole configuration within pentafluorobenzenethiol ((a): dipoles are facing downward to the substrate) and hexadecanethiol (c): dipoles are facing upward from the substrate). (b) and (d) are the charge, electrical field and potential within the pentafluorobenzenethiol and hexadecanethiol, respectively. The difference of potential on the top of the two thiols ($|\phi_1 - \phi_2|$) with respect to Au is estimated to be 0.4-1.1 eV.

4.3.5 Effects of dipoles on the surface energy and band alignment

When a thiol layer is deposited on Au surface, the surface dipole has two components: the Au-S dipole layer and the dipole layer within the thiol molecules. These dipoles change the surface potential and thus the effective work function of metal.[9] The surface potential shift has the form:[120] [121] [122] [4] [77] [123]

$$\Delta\phi = N(\frac{\mu_{metal^+S^-}}{\epsilon_0} + \frac{\mu_{mol,\perp}}{\epsilon_0\epsilon}) \tag{4.2}$$

where $\Delta\phi$ is the surface potential shift due to a dipole layer, N is the areal density of molecules, $\mu_{metal^+S^-}$ is the dipole moment of the metal-S bond, $\mu_{mol,\perp}$ is the thiol molecule dipole moment projected to the surface normal direction, ϵ_0 is the vacuum permitivity and ϵ is the relative dielectric constant of the thiol molecules. Studies suggest a covalent metal-S bond with a small intrinsic dipole in the self-assembled thiol monolayers on Au and thus the surface potential shift due to the metal-S interaction is small, between +0.02 eV to -0.05 eV.[123] It is also expected that the $metal^+S^-$ dipole, if any, has the same value for different

thiol SAMs.[120] The dipole configuration/direction is shown in Fig 4.13 (a) and (c) for pentafluorobenzenethiol and hexadecanethiol respectively. The pentafluorobenzenethiol has dipoles facing downward due to the more electronegative F atoms on the top, with normal-axial dipole moment of 1.33D.[124] [125] [126] [127] The hexadecanethiol has dipoles facing upward from the surface,[123] [120] with the normal-axial dipole moment of 1.5D.[123] Fig 4.13 (b) and (d) are the charge, electrical field and potential with respect to Au underneath within the two thiols, respectively. We assume N is about 1-2 $\times 10^{14}$ cm^{-2} and ϵ is around 2-3. According to the equation 4.2, the surface potential difference $|\phi_1 - \phi_2|$ in the two thiols is about 0.4-1.1 V, consistent with the overall shift of both the C 1s core level and valence band for the pentacene deposited on top. The shift of peaks is not present in NEXAFS because the NEXAFS spectra measure the energy difference from C 1s states to LUMOs, both of which are equivalently affected by surface potential change.

The band structure of the thiol/pentacene system is shown in Fig 4.14. Studies have shown that fluorinated thiols increase the surface work function by 0.5-1 eV, while alkane thiols slightly reduce the surface work function by 0.3-0.5 eV.[100] [11] [105] [106] [104] (schematically shown in Fig 4.14 (a)) The pentacene band structure on the right is from reference [77]. The effect of PFB and Hex thiol on the vacuum level is shown in the left part of (b) and (c). Based on the fact that PFB thiol has better charge injection and the HOMO measurements above, we think there is a band bending at the interface between pentacene and PFB thiol, pulling closer the HOMO to the Fermi level. In order to make this happen, certainly there are some charge transfer between pentacene and the thiol treated gold as in any Schottky diode configuration. When pentacene is deposited on the pentafluorobenzenethiol treated Au surface, the Fermi energies align by an electron transfer from pentacene to PFB/Au. This electron transfer is from the weakly bound HOMO state, and does not represent a chemical bond, which would produce inequivalent C atoms. The change of work function of thiol treated Au leads to a different energy alignment with pentacene. The hole injection barrier is ≤ 0.1 eV for pentacene/PFB/Au and ~ 0.5 eV for pentacene/Hex-thiol/Au, which are derived from HOMO XPS data (Fig. 4.9). The study of the vacuum level of thiol/Au upon the deposition of pentacene will be valuable to further understand the alignment of vacuum level and such study is underway using UPS.

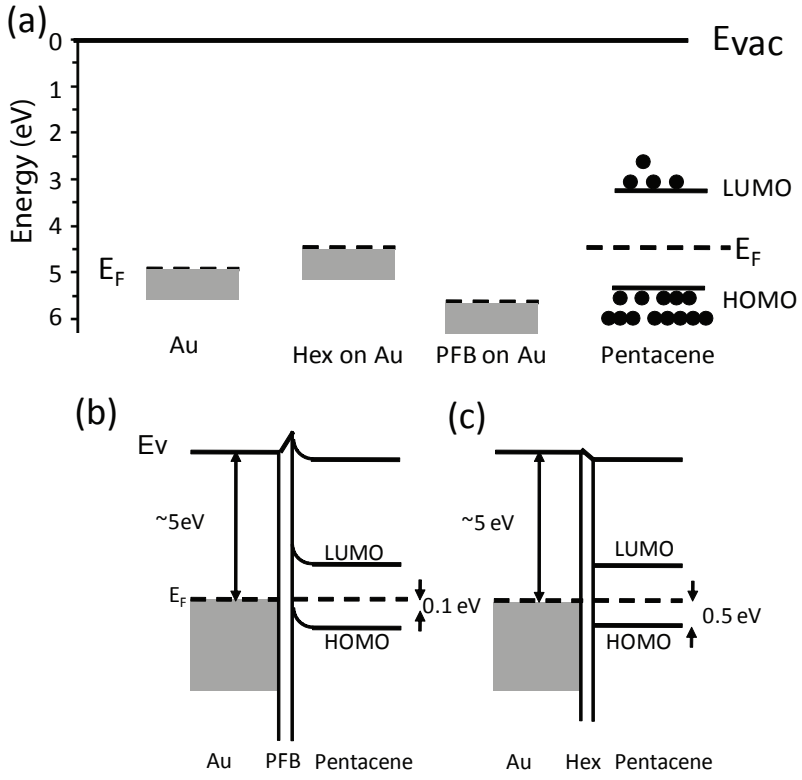

Figure 4.14: The energy level model proposed for Au/thiol/pentacene system. In (a), various samples are independently aligned with the vacuum level. Pentafluorobenzenethiol increases the work function of the Au surface, while hexadecanethiol slightly decreases the work function of the Au surface. (b) and (c) are bands alignments estimated based on the discussion for pentacene/PFB/Au and pentacene/Hex-thiol/Au samples, respectively, in the text. PFB/Au has improved hole injection barrier as indicated.

4.4 Conclusions

Electrical measurements of pentacene-based OFETs prepared with thiol treated contacts in the literature have shown improved device performance. By comparing an Alkane thiol (1-hexadecanethiol, Hex-thiol) and a fluorinated (thiol pentafluorobenzenethiol, PFB) layer using *in-situ* deposition, XPS, and NEXAFS measurement, we were able to directly observe interactions between the semiconductor and thiol-treated gold layers. HOMO XPS measurement demonstrated a smaller hole injection barrier into pentacene under PFB treatment when compared with Hex-thiol. NEXAFS measurements showed extra available states in the LUMO of the PFB treated device than the Hex-thiol device, indicating that electron density is donated by pentacene to PFB thiol to align their Fermi energies. Core-level XPS measurements and NEXAFS measurements indicated that no site-specific chemical reactions occurs between the thiols and the semiconductor. The NEXAFS measurements also demonstrate a standing-up morphology for both thiol treated samples, which has been demonstrated to lead to superior device performance.[101] We can, on the basis of these measurements, conclude that only morphological improvements lead to improved performance in the case of hexadecanethiol treatments, and both morphological improvements and a reduced charge injection barrier leads to improved performance in the case of pentafluorobenzenethiol treated contacts.

Chapter 5

Conduction model based on spatially variant mobility in OFETs

In organic field-effect transistors (OFETs), gate-voltage-dependent mobility [19] [128] and the study of trap residence time [22] [129] have suggested a trap-dominated charge transport mechanism. OFETs operate only in an accumulation mode where, according to the multiple trap-and-release model, the accumulated charges first fill deeper trap states, and eventually shallower states whose carriers are weakly bound. These carriers can be thermally activated from shallow states and move quickly from one trap site to another under electric field. However, the accumulated charges are not evenly distributed along the channel especially when the OFETs are operated in the saturation region, where the drain side has much less accumulated charges than the source side due to the cancellation of effective gate voltage by the drain voltage. Thus the carriers should be less mobile on the drain side where the trap states are filled less adequately, and one should expect a varied mobility across the channel. For the same reason, the saturation current formula $I_{DS} = \frac{W}{2L}\mu C_i(V_{GS} - V_{th})^2$ for silicon MOSFET is not suitable for OFETs, and thus the mobility calculation based on linear fitting of $\sqrt{I_{DS}}$ to V_{GS} is problematic. In this chapter, I review some prior work on correctly modeling linear mobility of OFETs. I also present the work of spatially resolved mobility modeling in the saturation region.

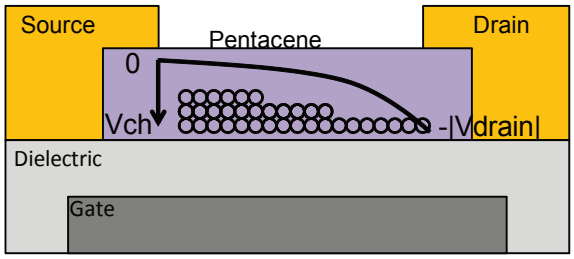

Figure 5.1: In saturation operation regime, charges are not evenly distributed along the channel due to the cancellation of effective gate voltage on the drain side by the channel voltage.

5.1 Prior art and the problem

As shown in chapter 1, for any position y along the channel, the drain current is

$$I_{DS}(y) = \frac{dV_{ch}(y)}{dy}\mu QW \tag{5.1}$$

where W is the channel width, $\frac{dV_{ch}(y)}{dy}$ is the electrical field along y in the channel, μ is the effective mobility, Q is the capacitive charge density and $Q = (V_{GS} - V_{th} - V_{ch})C_i$ (V_{GS} is the gate voltage, V_{th} is the threshold voltage, C_i is the dielectric capacitance per unit area, V_{ch} is the channel voltage and is a function of position y)

Integration of (5.1) in the linear region over channel length L and source-drain voltage V_{DS} results in

$$I_{DS} = \frac{W}{L}\mu C_i(V_{GS} - V_{th} - \frac{V_{DS}}{2})V_{DS} \tag{5.2}$$

Mobility can be extracted by fitting the I_{DS} vs. V_{GS} curve in the linear region under very small drain voltage, e.g., V_{DS}= -0.1 V.

However, the above integration works under the assumption that the mobility is constant and can be taken out of the integration, which is a valid approximation in the linear region but not in the saturation region. When the OFETs are operated in the saturation region, the accumulated charges are not evenly distributed along the channel (Fig. 5.1), where the drain side has much less accumulated charges than the source side due to the cancellation of

effective gate voltage by the channel voltage. Recall OFETs operate only in an accumulation mode where, according to the multiple trap-and-release model, the accumulated charges first fill deeper trap states, and eventually shallower states whose carriers are weakly bound. Thus the carriers should be less mobile on the drain side where the trap states are filled less adequately, and one should expect a varied mobility across the channel. For the same reason, the saturation current formula $I_{DS} = \frac{W}{2L}\mu C_i(V_{GS} - V_{th})^2$ for silicon MOSFET is not suitable for OFETs, and thus the mobility calculation based on linear fitting of $\sqrt{I_{DS}}$ to V_{GS} is problematic. The last section of this chapter tries to give out a solution to this problem by modeling the OFETs performance by a spatially resolve mobility.

5.2 Linear mobility calculation by quasi-static capacitance-voltage (QSCV) measurement

We have applied the QSCV method by Ryu,[130] to calculate the mobility in linear region of the OFETs with BT/parylene gate dielectric mentioned in chapter 2. The principle of derivation of mobility based on QSCV can be explained as following. In an OFET, the mobility can be extracted from the fundamental relationship:

$$\mu = \frac{v}{E}; v = \frac{I_{DS}}{WQ}; E = \frac{V_{DS}}{L} \tag{5.3}$$

where v is the velocity, $E$is the electrical field, W is the channel width, L is the channel length, and Q is the induced charge per channel area.

$$Q = \int_{+\infty}^{V_{GS}} (\frac{C_{ch}}{WL})dV; C_{ch} = C_{OFET} - C_{dep} \tag{5.4}$$

where C_{ch} is the channel capacitance due to the charge induced in the pentacene semiconductor, C_{OFET} and C_{dep} are the capacitance of the OFET under different gate voltages and completely depleted OFET. Both the values can be obtained from independent quasi-static C-V (QSCV) measurements (Fig.5.2 inset). Thus we have:

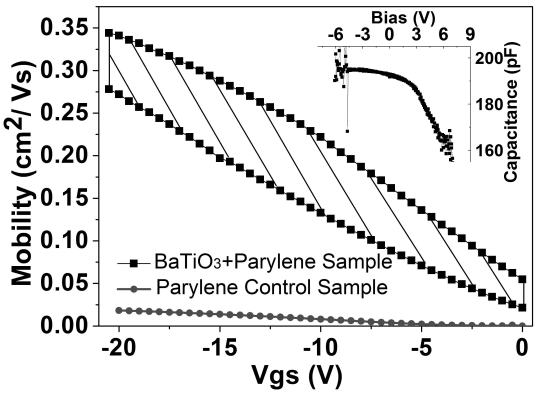

Figure 5.2: Linear mobility in OFETs with 110nm parylene only (dots) as gate dielectric and the ones with $BaTiO_3$/parylene (squares) as gate dielectric. The capacitance of 110nm parylene-C is 25 nF/cm^2, and that of the composite dielectric is 31 nF/cm^2. The inset: QSCV of $BaTiO_3$/parylene OFET.

$$\begin{aligned} \mu &= \frac{I_{DS}}{WQ} \cdot \frac{L}{V_{DS}} \\ &= \frac{I_{DS}L^2}{V_{DS}} / \int_{+\infty}^{V_{GS}} C_{ch} \cdot dV \end{aligned} \tag{5.5}$$

Using the transfer characteristic in the linear region, the mobility (squares) of $BaTiO_3$/parylene OFETs was calculated versus gate voltage (Fig.5.2) according to (1) and (2). For comparison, the mobility (dots) for OFETs with parylene only as gate dielectric was also drawn. The mobility in both cases had a strong dependence on the gate voltage. At V_{GS}=-20V, the mobility for OFETs with the $BaTiO_3$/parylene-C gate dielectric was ~ 0.35cm^2/(Vs), one order of magnitude larger than that in OFETs with parylene-C only as gate dielectric, which was ~ 0.03cm^2/(Vs). Assuming the mobility of the former can be extended to further negative gate bias in a linear scheme without any saturation, the value of mobility at V_{GS}=-40V is around $0.6 \sim 0.7$cm^2/(Vs).

5.3 Photocurrent method for measuring linear mobility

In equation (5.1), we have the drain current:

$$I_{DS}(y) = \frac{dV_{ch}(y)}{dy}\mu QW \tag{5.6}$$

Similarly, in a thin region of the channel exposed to the illumination beam at position y, photocurrent I_{PC} is:

$$I_{PC}(y) = \frac{dV_{ch}(y)}{dy}\mu(y)Q_{PC}W \tag{5.7}$$

where Q_{PC} is the surface concentration of photo-generated carriers in the exposed channel region, and is independent of gate voltage or position [83]. Integrating equations (5.6) and (5.7) in linear region (where mobility is seen as constant along the channel), we have:

$$I_{DS} = \frac{W}{L}\mu C_i(V_{GS} - V_{th} - \frac{V_{DS}}{2})V_{DS} \tag{5.8}$$

$$I_{PC} = \frac{W}{L}\mu Q_{PC}V_{DS} \tag{5.9}$$

Fig. 5.3 (a) is the gate-voltage dependence of source-drain current (open triangles) and photocurrent (open circles) of an air-free parylene-dielectric FET device operated under $V_{DS} = -0.1V$ (linear region), with respective fitting curves (solid lines). In the linear region, the source-drain current has a dependence of $|V_{GS} + 1.55(\pm 0.06)|^{2.21(\pm 0.02)}$ and the photocurrent has a dependence of $|V_{GS} + 1.05(\pm 0.06)|^{1.20(\pm 0.01)}$. The result, except for a difference of the threshold voltages in source-drain current and photocurrent, is consistent with equations (5.9) and (5.8), where one more order of V_{GS} dependence is expected for source-drain current than photocurrent, assuming n_{PC} is independent of V_{GS}. The result also implies that the mobility in the linear region increases with gate bias in the form of $\mu_{FETlinear} \sim V_{GS}^{1.2}$, consistent with Ryu's work [130]. In the saturation region, however, no simple relation can be derived.

Fig. 5.3 (b) is the gate-voltage dependence of source-drain current (open triangles) and photocurrent (open circles) of the same FET device operated under $V_{DS} = -15V$

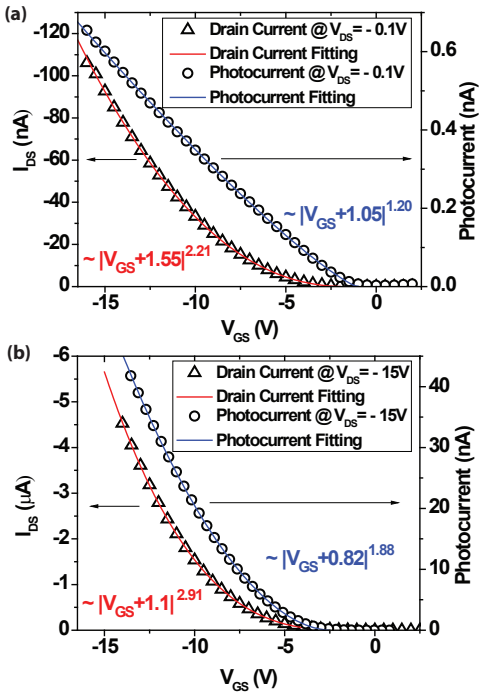

Figure 5.3: The gate-voltage dependence of source-drain current (open triangles) and photocurrent (open circles) of an air-free parylene-dielectric FET device operated in the linear region (a) and in the saturation region (b) with the whole channel under white LED illumination.

(saturation region). Fitting of the data shows that the source-drain current has a gate-voltage dependence of $|V_{GS} + 1.1(\pm 0.1)|^{2.91(\pm 0.04)}$ and the photocurrent has a dependence of $|V_{GS} + 0.82(\pm 0.09)|^{1.88(\pm 0.02)}$. In saturation region, the channel voltage V_{ch} at position y in the channel is: $V_{ch} = (V_{GS} - V_{th}) - \sqrt{(V_{GS} - V_{th})^2 - 2(V_{GS} - V_{th} - V_{DS}/2)V_{DS}(y/L)}$. If we approximate $V_{DS} = V_{GS} - V_{th}$, then $V_{ch} = V_{GS}(1 - \sqrt{1 - y/L})$. With the definition of an average mobility $\mu_{\bar{FET}}$ along the channel, $\mu_{\bar{FET}} = (\int_0^L \mu_{FET} dy)/L$, integration of (2) gives $I_{DS} = W/(2L)\bar{\mu}C_i(V_{GS} - V_{th})^2$. So Fig. 5.3 (b) indicates that the gate dependence of the average mobility in saturation region is approximately $\mu_{\bar{FET}} \sim V_{GS}^{0.9}$.

5.4 A new model of OFETs transport based on spatially resolved photocurrent measurement

Photocurrent response is a nondestructive method to probe the energy states [81] [80], interface properties [97] and mobility[83]. I have shown that photocurrent intensity is proportional to mobility in the linear region [97]. We extend this technique to the study of spatially resolved photocurrent [131] in OFETs operated in saturation region whose channel is exposed to a thin-beam light. Based on our model, spatial photocurrent measures locally the product of field and mobility, which can be used to elucidate the local mobility along the channel.

5.4.1 Spatially resolved photocurrent measurement setup

Pentacene OFETs with a parylene-C gate dielectric are fabricated on glass substrates using a bottom-gate, top-contact structure (Fig. 5.4). Photo-lithographically defined ITO patterns on glass are used as transparent gate. A blanket layer of 190-nm parylene-C as a gate dielectric is deposited in a custom chemical vapor deposition (CVD) system. 25 nm of pentacene is vacuum evaporated through a shadow mask at a rate of $0.1 \sim 0.2$ A/s with the substrate held at room temperature at a pressure $< 2\times10^{-7}$ Torr. Au source and drain contacts are then thermally evaporated also using shadow masking. With the transistors (channel length of 160 μm and width of 1000 μm) biased using a Keithley 2602 two-channel source/measure unit, the photocurrent was generated using a 633 nm He-Ne laser source

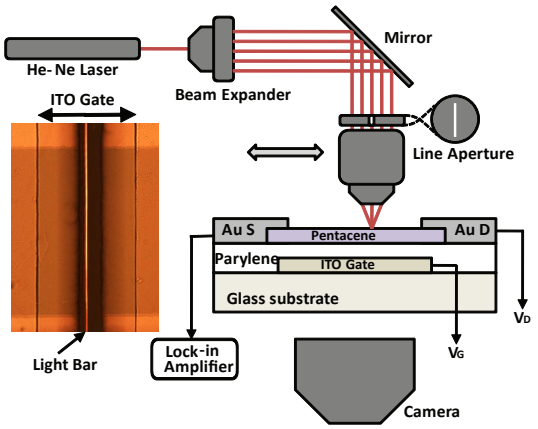

Figure 5.4: The experimental setup for spatial photocurrent measurement. The inset is a microscopic image of the channel region of a pentacene field-effect transistor. The line-shape beam is scanning across the channel while the photocurrent is taken.

expanded by a Gaussian beam expander. A 5 μm wide line aperture and a 10 $\times$ objective lens are used to focus a line-shape beam with a width of a few microns in the channel area, with the beam parallel to the channel width (as shown in the microscopic image inset in Fig. 5.4). The mirror, aperture and lens are mounted to a motorized linear stage so that the beam can scan across the channel. The photocurrent was measured using a Signal Recovery 7265 lock-in amplifier with frequency locked to 71 Hz while the laser beam was mechanically chopped.

5.4.2 Spatially resolve mobility measurement by photocurrent

Fig. 5.5 (a) is the spatial photocurrent in linear region from an OFET under V_{GS}= -20 V and V_{DS}= -0.5, -1, and -5 V, respectively. The photocurrent curve of V_{DS}= -5 V is divided by a factor of 2.5.

We model photocurrent similarly to drain current as stated previously. In a thin region of the channel exposed to the illumination beam at position y, photocurrent I_{PC} is:

$$I_{PC}(y) = \frac{dV_{ch}(y)}{dy}\mu(y)Q_{PC}W \tag{5.10}$$

where Q_{PC} is the surface concentration of photo-generated carriers in the exposed region,

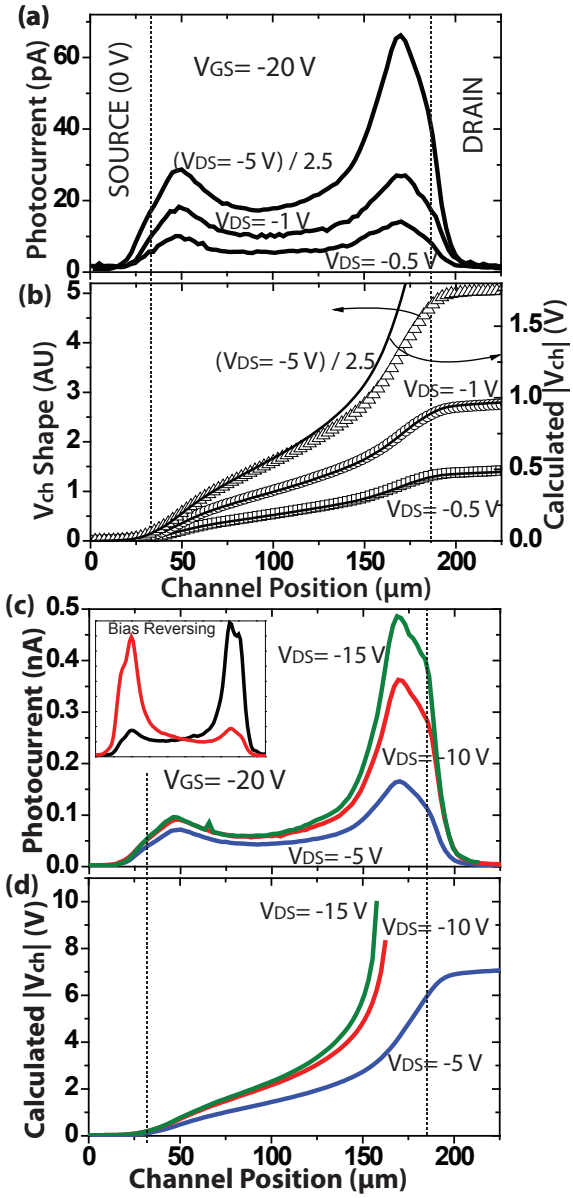

Figure 5.5: (a) Spatial photocurrent under V_{GS}=-20 V and V_{DS}=-0.5, -1 and -5 V, respectively. (b) Integration of spatial photocurrent in (a) over the channel length (open symbols) and calculated channel voltage (solid lines). (c) Spatial photocurrent under V_{GS}=-20 V and V_{DS}=-5, -10 and -15 V. The inset is the photocurrent curves of a different device under V_{gate}= -20 V, $V_{LeftMetal}$= -20 V / 0 V and $V_{RightMetal}$= 0 V / -20 V. (d) Corresponding calculated channel voltages.

and is independent of gate voltage or position [83].

In the linear region of operation ($V_{DS} = -0.5$ and $-1V$), the photocurrent is relatively level across the channel due to constant mobility and field. With increasing V_{DS} the photocurrent becomes increasingly asymmetric and the peak at drain side is significantly higher than that at the source side. According to (5.10), this increase of photocurrent at the drain side is due to the field increase (change of dV_{ch}/dy) at the drain side when the operation mode transitions from the linear to the saturation region. The two broad peaks at the source and drain contacts even when source-drain voltage is very low are attributed to the field increase by contact resistance.[132] [133] This can be compensated for in the linear region by placing a lumped or distributed contact resistance as a lower mobility region $\mu(y)$ at or near $y = 0$ and $y = L$. It would be desirable to use this method to quantify the contact properties especially the length scale over which the contact voltage drops [134] and the grain disruption near the contact edge in bottom contact devices. However, the laser beam is not focused tightly enough using the projection optical system we built to localize the contact area, and significant shadowing of the broad beam by the contact also introduces errors in the measurement. Work to address both of these limitations is now underway.

In linear region, μ is independent of position, and the integration of $I_{PC}dy$ in (2) should result in:

$$V_{ch}(y) = \frac{1}{\mu Q_{PC} W} \int_0^y I_{PC} dy \tag{5.11}$$

By combining this with a measurement of the mobility or field taken in the linear region (using, for example, the approach proposed in [130] or scanning potentiometry), it is possible to calibrate the photoresponse to the local effective mobility. The integration of measured I_{PC} from position 0 to position y in the channel $\int_0^y I_{PC} dy$ is plotted as open symbols (squares, circles and triangles under drain voltage of -0.5, -1 and -5 V, respectively) in Fig. 5.5 (b). Because of the difference between integrating step and the width of excitation beam, the above integration holds the shape for V_{ch} with an arbitrary unit.

In the saturation region, however, both the field and mobility in (5.10) are functions of position. Potentiometry can be used to measure $V_{ch}(y)$ and thus dV_{ch}/dy, so that μ can be derived from (5.10). Here we provide an alternative means to obtain local mobility. The

general idea is to produce a mapping between the mobility and channel charge in the linear region, where mobility can be determined more precisely, and use this mapping to derive the local mobility in saturation region.

Linear mobility can be extracted by fitting the I_{DS} vs. V_{GS} curve in the linear region under V_{DS}= -0.1 V. Dielectric capacitance is measured by quasi static capacitance-voltage measurement [130]. For this particular device, our result shows that mobility follows:

$$\mu_{linear} = \mu(Q) = \mu_0(V_{GS} - V_{th})^{1.34} \tag{5.12}$$

where μ_0 is 7.58×10^{-4} and V_{th}= -9.5 $\pm$ 0.5 V (the resulted μ_{linear} is in cm^2/Vs) for this particular device.

We propose that the local mobility in saturation mode at position y has the same dependence on capacitive charge as in the linear region:

$$\mu_{sat}(y) = \mu(Q) = \mu_0(V_{GS} - V_{th} - V_{ch}(y))^{1.34} \tag{5.13}$$

Putting (5.13) into (5.10) and integrate: $\int_0^y I_{PC}dy = A\int_0^{V_{ch}(y)}(V_{GS} - V_{th} - V_{ch})^{1.34}dV_{ch}$ (where A is a constant) which results in:

$$\int_0^y I_{PC}dy = A'[(V_{GS} - V_{th})^{2.34} - (V_{GS} - V_{th} - V_{ch})^{2.34}] \tag{5.14}$$

where A' is a constant consisting of W, Q_{PC} and the ratio between the photocurrent per integrating step and photocurrent measured over the width of excitation.

To confirm our hypothesis, we calculated the channel voltage in the linear region. A' can be estimated using I_{PC} data under V_{DS}= -0.5 V, knowing that at the drain contact V_{ch}= -0.5 V. Using the estimated A' (=0.055), V_{ch} can be obtained through (5.13) in the linear region as plotted as solid lines in Fig. 5.5 (b). It shows that for V_{DS}= -0.5 V and V_{DS}= -1 V, the calculated curves of V_{ch} follow well with those of $\int_0^y I_{PC}dy$ in shape and the calculated V_{ch} is close to 1 V at the drain side under V_{DS}= -1 V. For V_{DS}= -5 V, however, the calculated V_{ch} does not match $\int_0^y I_{PC}dy$ in the region close to the drain electrode because the assumption of constant mobility - and thus (5.11) - is not valid in saturation.

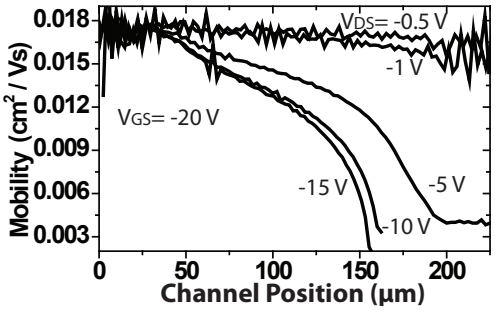

Figure 5.6: Calculated mobilities along the channel using eq (2) under V_{GS}= -20 V, V_{DS}= -0.5, -1, -5, -10 and -15 V respectively.

Fig. 5.5 (c) is the spatial photocurrent from the same device under V_{GS}= -20 V and V_{DS}= -5, -10 and -15 V. The inset shows the photocurrent curves of a different device under V_{gate}= -20 V, $V_{LeftMetal}$= -20 V / 0 V and $V_{RightMetal}$= 0 V / -20 V. It is clear that the asymmetric shape of the photocurrent curve is not due to structure nonuniformity but the direction of the applied source-drain voltage. Channel voltage V_{ch} is calculated using (5.14) and shown in (d). The calculated channel voltage $|V_{ch}|$ at the drain is $\sim$ 7 V when the OFET is under V_{DS}= - 5 V due to the difference in accumulated error in the integration across the channel when compared with the reference V_{DS}= -0.5 V measurement. The measurement is not able to determine the potential using (5.14) in the pinched-off region where the charge carrier density is small.

Local mobility can be extracted from (5.10) after V_{ch} is obtained. In figure 5.6 are the calculated mobilities along the channel using (5.10) under V_{GS}= -20 V, V_{DS}= -0.5, -1, -5, -10 and -15 V respectively. The calculation shows almost constant mobility along the channel when the device is operated in linear region, which also matches the value calculated using (5.12). In the saturation region, the mobility decreases across the channel from source to drain due to the decreased density of carriers on the drain side.

To model the OFETs performance, a generalized method is summarized as following:

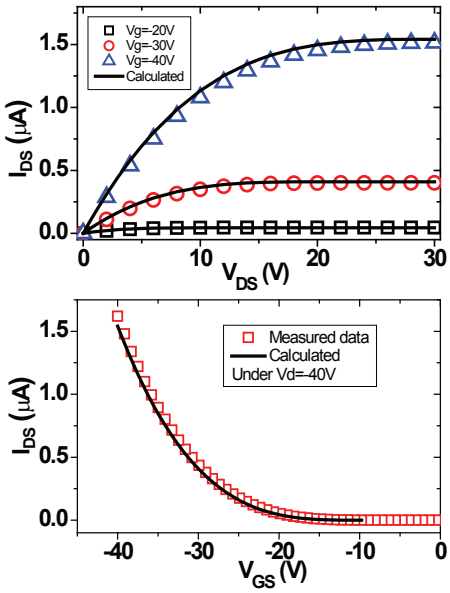

Figure 5.7: (a)I_{DS} vs. V_{DS} experimental data (symbols) and simulation (lines).(b)I_{DS} vs. V_{GS} experimental data (symbols) and simulation (line).

$$I_{DS}(y) = \frac{dV_{ch}(y)}{dy}\mu QW \tag{5.15}$$

$$Q = (V_{GS} - V_{th} - V_{ch})C_i \tag{5.16}$$

$$\mu_{linear} = \mu_0(V_{GS} - V_{th})^{\alpha} \tag{5.17}$$

$$\mu_{sat}(y) = \mu_0(V_{GS} - V_{th} - V_{ch}(y))^{\alpha} \tag{5.18}$$

$$\tag{5.19}$$

$$\int_0^L I_{DS}dy = \int_0^{V_{DS}} W\mu_0(V_{GS} - V_{th} - V_{ch})^{\alpha} \cdot (V_{GS} - V_{th} - V_{ch})C_i \cdot dV_{ch} \tag{5.20}$$

$$I_{DS} \sim ((V_{GS} - V_{th})^{\alpha+2} - (V_{GS} - V_{th} - V_{DS})^{\alpha+2}) \tag{5.21}$$

The calculation based on the above model is shown in Fig. 5.7

5.5 Conclusion

We have reviewed curve fitting method and QSCV method for deriving linear mobility in OFET. Because in OFETs the mobility varies with gate bias, the formula used in Si

MOSFET describing source-drain current in saturation region does not apply to OFETs. We have measured spatially resolved photocurrent in OFETs operated in the linear and saturation regions. Because the photogenerated charge is constant as a function of bias, spatially resolved photocurrent measurement locally measures the product of channel field and mobility. This product can be used to derive the local mobility across the channel. Our results directly show that in the saturation region, mobility decreases from source contact to drain contact due to the decreased density of carriers on the drain side.

Chapter 6

Conclusions and Future Work

6.1 Contribution of this work

This thesis has systematically discussed the two important interfaces in OFETs - the dielectric-semiconductor interface and the semiconductor-contacts interface. Specifically, it has explained how the dipole layer introduced during the dielectric surface treatment can affect the electrical performance; we have developed novel spectral photocurrent and $1/f$ noise spectroscopies to study the oxygen doping effect at the dielectric-semiconductor interfaces; we have studied the intentionally introduced dipoles and their contribution to the improvement of contacts by the combination of *in situ* deposition and synchrotron surface spectroscopic techniques; we have also demonstrated the use of high-dielectric-constant nanoparticles and functional polymer as gate dielectrics and shown the improvement of device performance and integration of new functionalities.

The characterization techniques developed in this thesis, such as spectral and spatial photocurrent, 1/f noise and high-energy spectroscopies, can also be applied to other organic electronics fields - solar cell, light emitting diodes, and various sensing applications.

Specifically, this thesis has demonstrated:

- that nanoscale high-κ materials which are normally ferroelectric can be used as gate dielectric where their high dielectric constant is desirable but ferroelectric hysteresis is not

- that spectral photocurrent and $1/f$ noise can be used to probe the doping effect at the interface of dielectric and semiconductor in OFETs
- that a novel spatially resolve photocurrent measurement can be used to measure position-variant local mobility in OFETs
- a model based on position-variant mobility to describe the electrical behavior of OFETs
- that surface dipole plays an important role in energy alignment between organic semiconductor and metal contacts
- the usage of synchrotron surface spectroscopies to study such energy alignment

6.2 Future works

The developed characterization techniques can be further improved and be applied to many other materials and devices. For example, $1/f$ noise can be used to monitor device degradation while the device is exposed to reactive agents and to study the trapping states associated with the degradation. A finer resolution for spatially resolved photocurrent measurement is necessary to clearly single out the contacts effect. The combination of spatial potentiometry and photocurrent can further confirm and improve our understandings of carriers behavior in the conduction channel. To apply the synchrotron surface probes to study oxygen doping effect at the dielectric-semiconductor effects would be ideal for people to understand the chemistry at the interface.

The contacts in organic thin film transistors are especially important and can cause significant complication for accurate characterization and modeling of transistors. In some cases the contact resistance is comparable to channel resistance even for long channel devices.[135] The contact resistance is Schottky barrier in nature. It changes with drain bias because the Schottky barrier changes height under different drain bias; it changes with gate bias because the gate-modulated carrier density in semiconductor will change the width of the Schottky barrier. Studies of such contact effect and exclude them from device characterization done in chapter 5 would be beneficial for a clearer understanding of OFETs

behaviors.

On the applicationary research side, there are many possibilities. Integration with functional organic materials under low thermal budget is an area that is potentially interesting for inexpensive large area applications. Force, vibration, touch and ultrasonic sensing over a large surface with flexible shape can be used in many robotic and human-machine interface applications.

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Appendix A

Laboratory evaporation systems for fabricating organic thin film devices

A.1 Introduction

Physical vapor deposition (PVD) and chemical vapor deposition (CVD) are two popular methods to process organics. For example, pentacene, a polycrystalline high mobility p-type semiconductor is often evaporated by PVD and mainly used in OFETs. Another example, parylene, a group of polymers based on poly-para-xylylene, provides excellent dielectric, encapsulation and surface treatment properties and conformally deposited through a unique CVD process. Commercially available deposition systems (*e.g.* from Kurt J. Lesker and Specialty Coating Systems) for these materials are costly and offer very limited customizability. Samples are usually transferred in air between systems and air-free fabrication and encapsulation is difficult.

We have developed relatively inexpensive, customized, and LabVIEW-automated PVD and CVD systems well suited for laboratory research purposes. The systems utilize computer control and relay-based power controllers. The deposition rate and power controller are linked in software instead of using expensive dedicated hardware such as a programmable

logic controller. The system easily integrates with a glove box, which minimizes exposure to oxygen and water during fabrication and encapsulation. Automation of film growth ensures a reliable and repeatable film quality. Many colleagues have requested detailed information of building these systems, and we believe a general report on how to build such systems will benefit many researchers in the organic and thin film device community.

A.2 Pentacene Thermal Evaporation System

A.2.1 Components and design

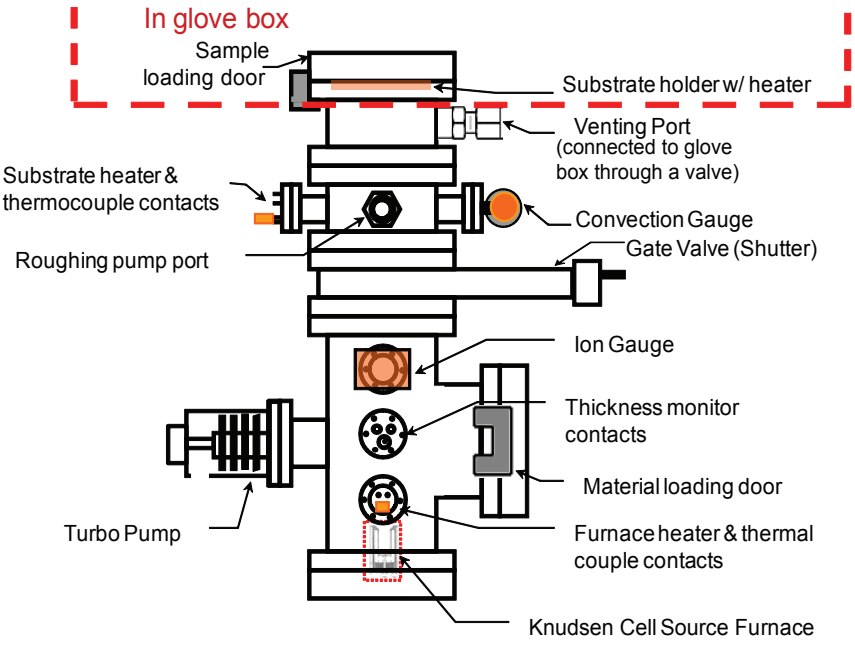


Figure A.1: Cross-section schematic of pentacene evaporation system.

A two-chamber configuration is adopted in pentacene evaporation system to increase the fabrication throughput. Figure A.1 is the cross section schematic. The top sample loading chamber includes an 8" ConFlat (CF) tube welded through the bottom plate of a glove box (red dotted line). It has a venting port that connects to the glove box through an external valve. The top chamber also has a tube with a rough pumping port, substrate heater/thermocouple feedthrough, and a convection gauge that measures pressure down to

mTorr. Studies have shown that pentacene transistor performance varies with substrate temperature during deposition. [24] [25] However, it is worth noting that the condition parameters (*e.g.*, substrate temperature and evaporation rate) are not exactly the same for each setup and some experimentation is required to determine the optimum conditions for a given deposition and material system. Bottom chamber includes evaporative source, turbo pump and ion gauge. A gate valve separates the two chambers and is also used as a manual shutter. Samples are placed on the top loading door facing downward. The resulted large working distance (> 25") is favorable for shadow masking patterns on sample. The gate valve always keeps the bottom chamber in high vacuum ($< 1e^{-7}$ Torr) while samples are loaded into the top chamber. A rotary pump functions as both the backing pump for the turbo and the roughing pump for the upper chamber. A three-way valve switches between the two functions. This design requires neither pumping whole chamber (except when refilling the source) nor waiting for the furnace to cool down before switching different samples, thus a high throughput can be achieved.

While this architecture can be used in air, the simplicity with which it can be integrated with a glovebox whose environment is scrubbed of water vapor and oxygen is of particular advantage for processing organic semiconductors. While pumping air, the majority of residual gas in a chamber is hydrodren and water vapor in the pressure range of 10^{-3} to 10^{-6} Torr. [136] A glovebox environment, which can maintain water vapor at a concentration below 0.1PPM, can significantly shorten the pumping time due to the lack of water and reduce exposure to residual gases that can decrease device performance. [24] For a routine operation, $\sim 1e^{-7}$ Torr vacuum can be easily achieved within 30 to 45 minutes after loading the sample. In a glovebox environment, the reaction of organic materials with reactive residual gases, most notoriously, water and oxygen, can therefore be suppressed before, during, and after deposition.

A.2.2 Evaporative source

There are generally two kinds of evaporative sources: nonequilibrium and quasiequilibrium sources. [137] A representative example of a nonequilibrium source is a folded metal boat made of W or Mo which can hold the source material open to the chamber. Upon heating,

the material evaporates over a large solid angle with little confinement from the boat. Heating is usually not uniform; the part of source material in contact with the boat is heated and evaporates first, which may induce the ejection of unmelted material on top (the popcorn effect).[1]

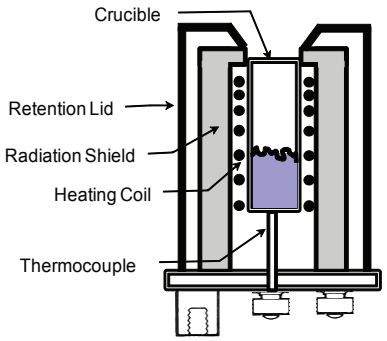


Figure A.2: Cross-section schematic of a modified Knudsen cell used as pentacene evaporative source.

An example of a quasi-equilibrium source is the Knudsen cell (K-cell), which is an isothermal enclosure with a small orifice. The source material is placed in the center crucible surrounded by the filament, the density of which is engineered so that the loss of heat at the top orifice is compensated by excessive heating. A radiation shield is wrapped around the filament to prevent radiative heat loss to the chamber. A modified Knudsen cell, can also be used, with a large opening relative to the crucible size (Fig. A.2). This arrangement retains the higher heating efficiency of a K-cell, but can also achieve directional deposition and higher material utilization efficiency than a boat source or K-cell.

A.2.3 Communication and control in LabVIEW

An essential component for realizing automation of the pentacene evaporation is the control of the source power in a way that the evaporation rate can be maintained and adjusted. Often this is done through integration of PID control and silicon control rectifier (SCR) circuits as shown in Fig. A.3. AC power supply is transformed usually to a low-voltage, high-current source which is connected to a SCR unit, which can adjust the output power

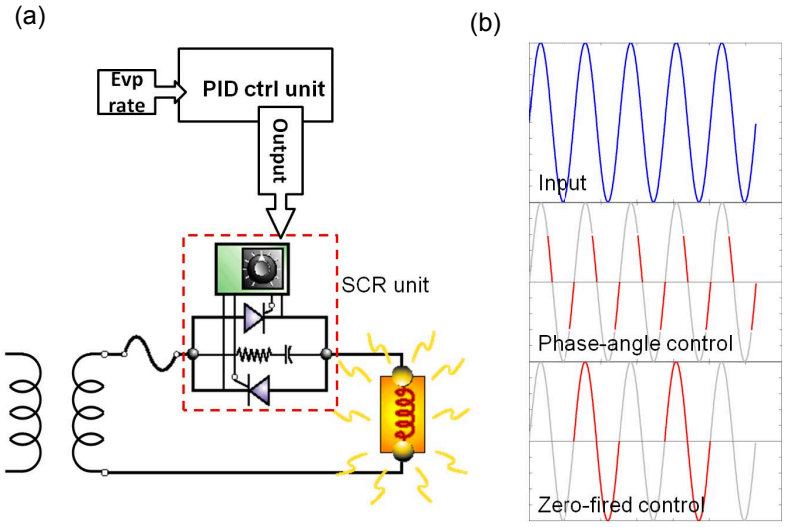


Figure A.3: (a) Most commercial systems adapt the integration of PID control and SCR circuit with an AC power supply to optimize the heating power to adjust/maintain evaporation rate. (b) Two operation modes for SCR circuit: phase-angle control and zero-fired control.

using the phase-angle control or zero-fired control schemes (Fig. A.3(b)).

In our pentacene evaporation system, software takes a big role in control and automation. The rate is monitored, controlled, and fed-back through LabVIEW, and the temperature of the furnace source adjusted for the optimum rate. The setpoint temperature is maintained using a PID temperature controller (*e.g.* the Delta DTB temperature controller) and using the built-in relay or a peripheral higher current relay controlled through duty-cycle adjusted digital output mode. Only a regulated DC power supply is needed and phase-fired silicon-controlled rectifiers (SCRs) and the complications associated with the inductance of step-down transformers can be eliminated.

The modified K-cell cell for pentacene evaporation is power efficient due to the heating architecture mentioned above, and operates at relatively low temperatures ($\sim$ 200 °C). Relatively little input power is needed to maintain the temperature, which ensures a relatively stable operation even driven by a regulated voltage source with a switching relay. It is worth noting that the heating filament is low in resistance ($\sim$ 0.7 ohm for a RADAK I from

LUXEL) and the resistance does not vary much ($< 5\%$) within the temperature range of 20 - 210 °C. Thus the external voltage source should have a low output voltage (*e.g.* 3.3 V) and a relatively high current limit (*e.g.* > 5 A for a 3.3 V power supply).

The linkage between evaporation rate (monitored by a USB interfaced crystal monitor) and the source heating power (adjusted by temperature controllers through "setpoint temperature") is established in LabVIEW. A simplified algorithm flowchart and a sample LabVIEW interface are shown in Fig. A.4 (a) and (b) respectively. The complete programs can be found on our website.[138] As the evaporation initiates, the system is first heated to a preheat temperature and then the furnace setpoint temperature is linked to the evaporation rate. If the evaporation rate is lower than the set rate, for example, the program simply increases the source setpoint temperature by a preset step. A time parameter controlling the frequency of changing the setpoint temperature in the source controller compares its value with "time elapsed" variable in LabVIEW. The appropriate setting of this parameter avoids the rate oscillations and its value depends on the source, power, PID settings and target temperature. For the pentacene system with typical operation source temperature of ~ 200 °C, the setpoint temperature needs only to be changed once per 10 seconds by a step of 0.5 °C. For a metal evaporation system with the similar configuration but with a target source temperature of 1300 °C, however, the setpoint temperature should be adjusted less than once per 3 seconds to avoid rate oscillations. More advanced PID control can also be implemented in LabVIEW.

A.3 Parylene Chemical Vapor Deposition (CVD) System

A.3.1 Components and design

Parylene is a class of polymer that originates from the basic form poly-para-xylylene (parylene-N). They are usually deposited through CVD process and forms conformal coatings on various surfaces. They offer good chemical and electrical barrier properties, and thus are applied as electronic coatings, encapsulants and dielectric materials. [139] [140] [141] [142] Many forms of parylene are commercially available offering different surface and dielectric properties such as gas permeability and dielectric strength. Parylene C substi-

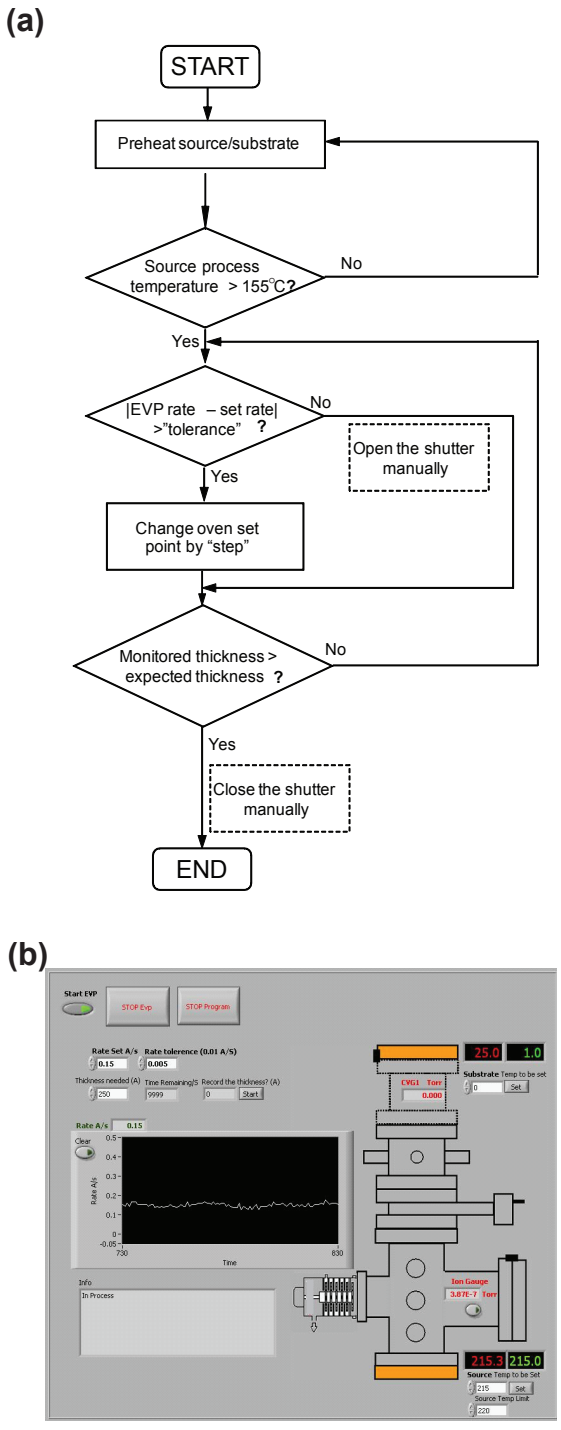


Figure A.4: (a) Pentacene evaporation control flow chart showing the algorithm for controlling deposition rate (b) A sample LabVIEW control interface.

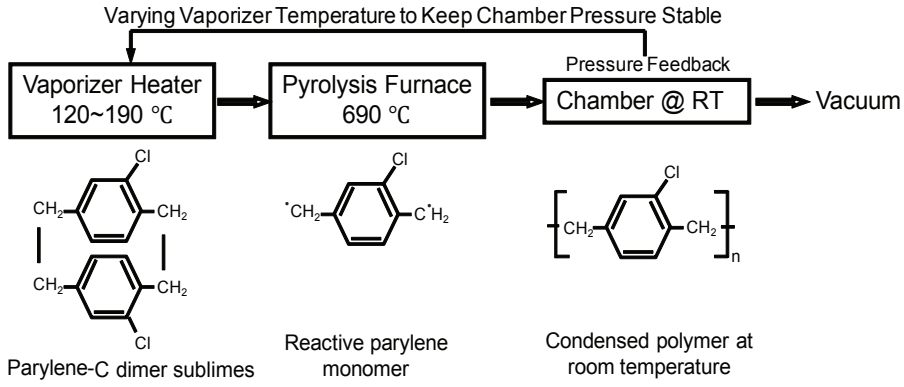


Figure A.5: Process of CVD deposition of parylene. Sublimed dimer vapor is pyrolyzed into reactive monomers. The monomers condense and polymerize on chamber and substrate surfaces held at room temperature.

tutes a chlorine atom for one of the aromatic hydrogens in parylene-N and offers higher dielectric constant and lower gas permeability for water vapor and oxygen than parylene-N. Pristine parylene-C film is hydrophobic and can be a robust dielectric layer [143] and surface treatment layer [33; 61] in organic thin film devices. Fig. A.5 illustrates the CVD process of depositing parylene-C. Commercially available dimer sublimes at around 120 - 190 °C and breaks into reactive monomers in the pyrolysis oven held at around 690°C. The monomers then condense and polymerize in the chamber held at room temperature and forms a conformal coating on the substrates.

Many organic thin film devices fabricated in glovebox need to be encapsulated before exposure to air. For some applications (*e.g.* surface treatment and dielectric layer) the thickness of deposited film needs to be monitored and controlled. Commercial systems do not provide such capabilities at low cost. We have develop a low-cost custom CVD system that is attached to a glovebox, where the fabricated organic devices (OLEDs, transistors, solar cells, etc) can be encapsulated without taking them outside the glovebox. A schematic cross section of custom parylene CVD is shown in Fig. A.6. The monomer is introduced into the chamber through a flute baffle with holes facing toward the chamber wall to achieve an even distribution of the monomer vapor. A rotational stage is essential for a uniform deposition. A vertical stack sample holder is used to hold multiple samples. The vaporizer

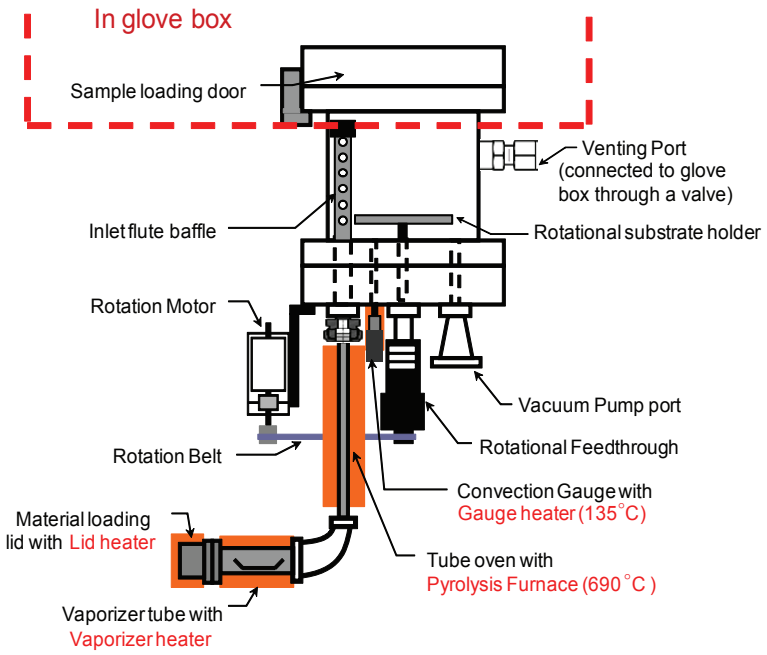


Figure A.6: A schematic of the custom parylene CVD cross section. The chamber is attached to the bottom of a glovebox and the lid opens in the glovebox. Water- and oxygen- free encapsulation and processing can be completed.

lid and vacuum gauge need to be heated to prevent parylene from depositing on them. The deposition is fully automated in LabVIEW. A control box consisting of temperature controllers (Delta DTB series) and relays connects, controls and monitors the temperature of vaporizer, pyrolysis furnace, lid and vacuum gauge heaters, and the chamber pressure.

A.3.2 Communication and control

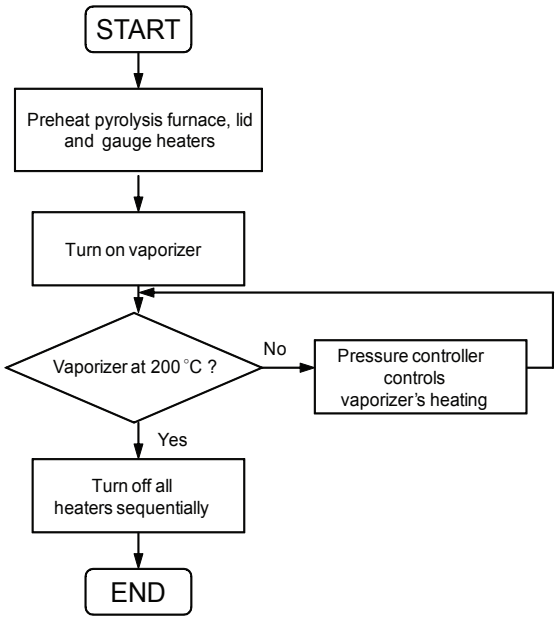


Figure A.7: Parylene CVD control flow chart. The pressure controller (analog read mode in a temperature controller) maintains the chamber pressure to a preset value by adjusting the output heating power using internal PID control algorithm. See text for details.

The control box communicates with LabVIEW through RS-485 serial communication. A simplified control flow chart is shown in Fig. A.7. The pyrolysis oven, lid heater and vacuum gauge heater are first heated to certain temperatures and kept at these temperatures. A temperature controller is used as a pressure monitor by changing the input mode into analog read from K type thermocouple mode. Once the vaporizer is on, the pressure controller maintains the system pressure to a preset value (10 - 30 mTorr) by adjusting the output

heating power using internal PID control algorithm. A constant pressure ensures a stable deposition rate and the rate is proportional to the deposition pressure. In our system, the deposition rate and film thickness are monitored by a crystal monitor (not shown in Fig. A.6). If the deposition thickness is not critical, the thickness can also be roughly controlled by adjusting the amount of dimer material loaded. With the amount of material decreasing, the vaporizer gradually increases the heating temperature to keep the pressure constant. Eventually the vaporizer's temperature will rise to a certain point indicating the source material is gone and the evaporation is finished. All the LabVIEW control VIs can be found on our website. [138] It is worth noting that the control can be fully realized without a computer and LabVIEW, but through the use of programmable logic circuit (as in commercial systems) and Arduino, which is a widely used open source hardware platform with series communication capability.

A.4 Cost and ordering information

We provide some ordering suggestions in table A.1for the parylene CVD system. The vacuum parts are easily accessible from major vendors. A welded integrated part for the vaporizer tube, the pyrolysis tube and the elbow tube between them can be custom ordered from Sharon Vacuum. Low speed motor can be found from McMaster for $ 50. We recommend RIGAKU Model 10C-99011500 for the rotational feedthrough. Pipe heaters for the lid and vaporizer, tape heater for the vacuum gauge and ceramic heater for the pyrolysis tube can be found from watlow, McMaster, etc. A liquid nitrogen trap between the chamber and the vacuum pump is needed to trap parylene waste and can be ordered from Lesker.

Table A.1: Pentacene system parts order information and costs

Item	Vendor/Product	Price $
Source Heater	LUXEL/RADAK I vacuum furnace	3600
Power Supply	TRC electronics/RS-50-3.3	30
Temperature Controller	Factorymation/Delta DTB RR	80
Vacuum Pump Station	Pfeiffer/HiCube Eco Turbo Station	5000
Vacuum Chambers	Sharon Vacuum cutom	3100
Thermocouple & feedthrough	MDC, Lesker, Huntington, etc	500
Gate Valve	MDC, Lesker, LDS vacuum, Huntington, etc	2000
2 Doors	Huntington vacuum	1600
Crystal Monitor	Inficon/932-000 sensor head;	1400
	930-004 feedthrough; Q-pod controller	
Gauge	Instrutech/	1500
	IGM 402 Ion Gauge with convection gauge	
Others		1000
Sum		19810

Appendix B

Active-matrix force sensing and actuators based on piezoelectric and electrostrictive polymers

B.1 Force sensing based on piezoelectric polymer

PVDF piezoelectric polymer film generates charge under mechanical stimuli. In Fig. B.1, the piezoelectric coefficient in direction 3 (thickness direction) is defined as:

$$d_{3j} = \frac{Chargedensity}{Appliedstress} = \frac{Q_3/A_3}{F_j/A_j} \tag{B.1}$$

where j is the direction of mechanical excitation/actuation. For PVDF film, $d_{31} = 23$ C/N and $d_{33} = 23$ C/N.

The design of a sensing element is shown in Fig. B.2.[144] Here the FET acts as a dimer; the charge generated by PVDF will induce charges in the channel and thus modulate the drain current of FET. The OFET converts the charge signal into current; this conversion overcomes the problem of charge sharing over various transmittance capacitance (e.g., wires) that happens in voltage/charge transmitting.

The completed sensing device is laminated on a PVC card and the PVC card is cycled between bending and releasing. The identical force exerted on the sensing device is stretching along the channel width direction (Fig. B.3 (a)). Fig. B.3 (b) shows the current

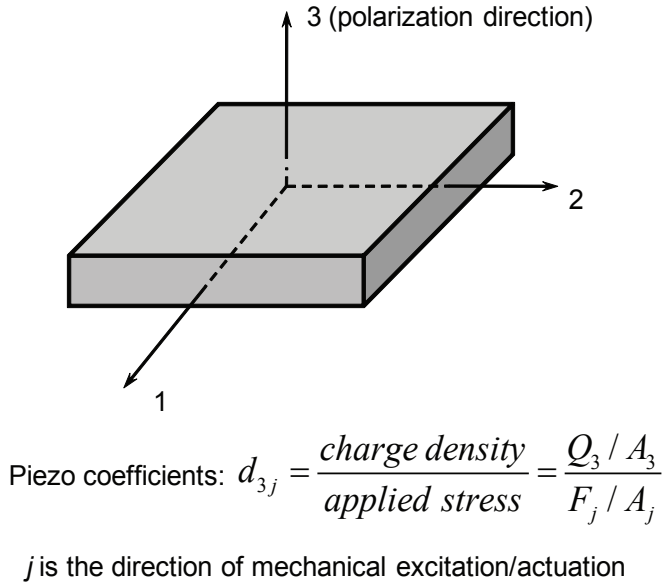


Figure B.1: Piezoelectric coefficient definition

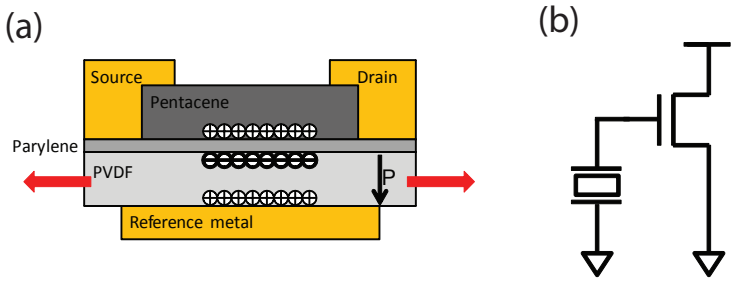


Figure B.2: Structure of OFET directly fabricated on PVDF film and its circuit representation.

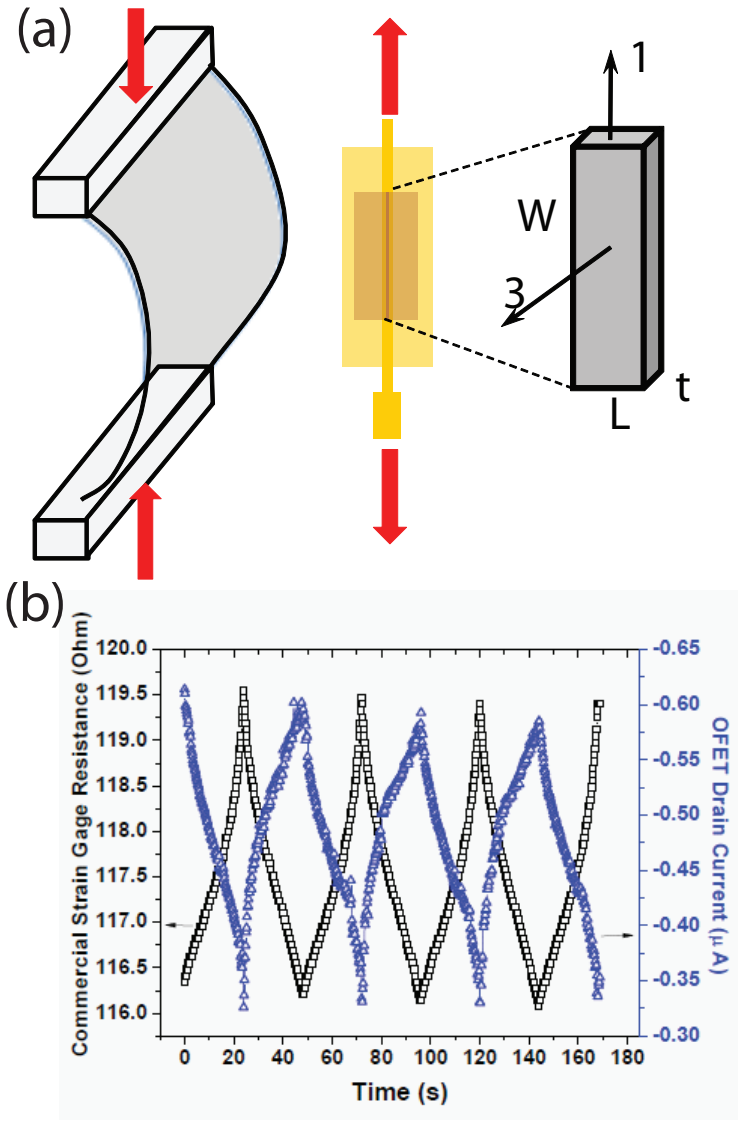


Figure B.3: (a)The testing structure of the sensing element. The modulation of drain current is shown in (b).

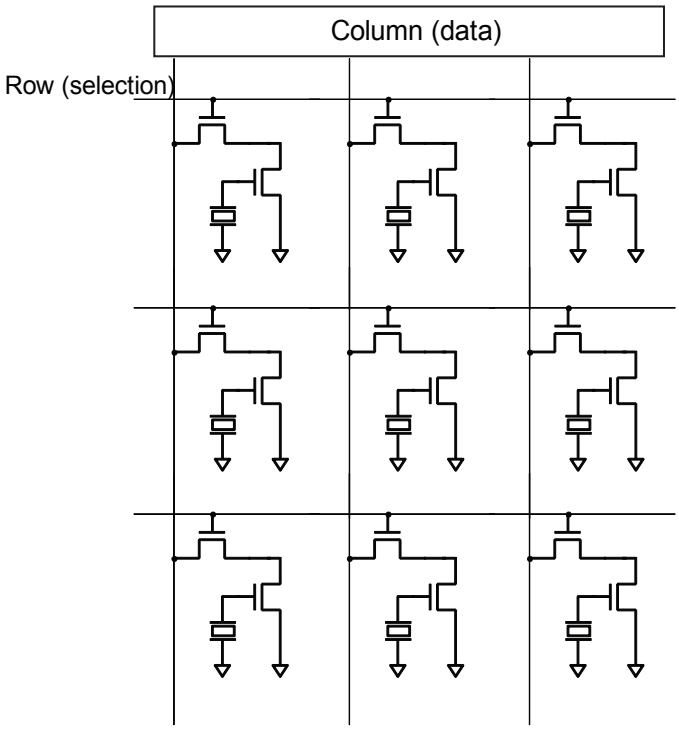


Figure B.4: The active matrix structure can be realized by adding one transistor in each sensing element

modulation of a FET (right y axis) and the resistance change from a commercial resistive strain gauge (left y axis).

The active matrix structure can be realized by adding one transistor in each sensing element (Fig. B.4). Active matrix structure has improved scalability and speed.

Alternatively, the sensor and the OFET can be separate and coupled through a connected gate metal.[145][146] Fig. B.5 shows the different designs. For the characterization of the sensing element, ideally an output linearity (output vs. applied force under fixed excitation frequency) and frequency response (output vs. frequency under fixed force) are obtained.

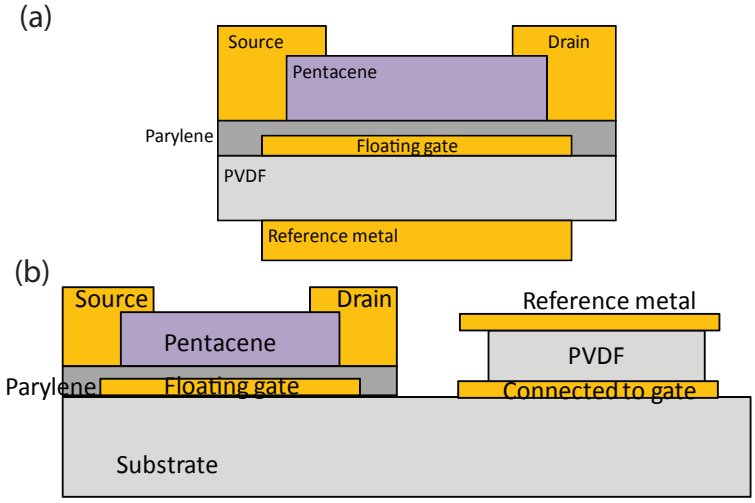


Figure B.5: Two alternative designs for OFETs and PVDF coupling through a floating gate metal.

B.2 Active-matrix actuators based on electrostrictive polymer thin film

As mentioned in chapter 2, P(VDF-TrFE-CFE) terpolymer can be used as electrostrictive actuators. Compared to its ferroelectric material version P(VDF-TrFE), the terpolymer has a key advantages - no hysteresis during polarization. Substantial energy is wasted when switching the ferroelectric film polarization. By adding the -CFE imperfections into the polymer, the long range correlation between polar groups is broken. The Curie point is brought down below room temperature; thus the material exhibits mainly paraelectric phase at room temperature. The ferroelectric and paraelectric configurations are shown in Fig. B.6.[13] -CFE is not shown in the plot. At room temperature, the alternating trans-gauche configuration that is non-polar is dominant. Under an electrical field, the polar molecules align with the field within one polymer segment and form the all trans conformation in (a). The addition of -CFE significantly reduces the energy barrier for the phase transformation of para- and ferro-electric phases, and thus eliminates the hysteresis. As seen in Fig. B.6, this phase transition associates with large molecular conformation changes, leading to very large macroscopic deformation (and thus large electrostrictive ef-

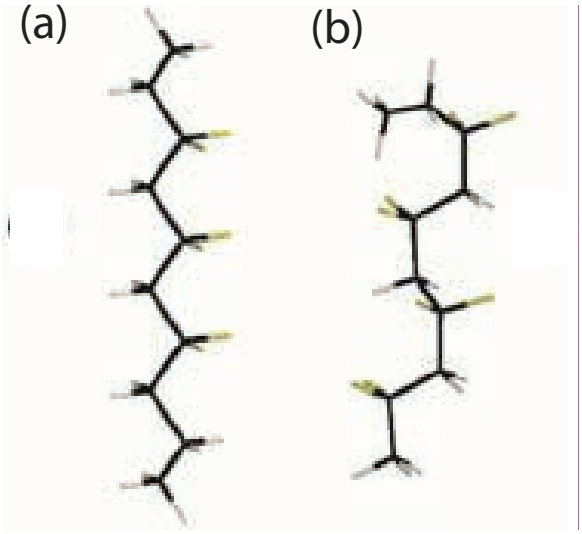
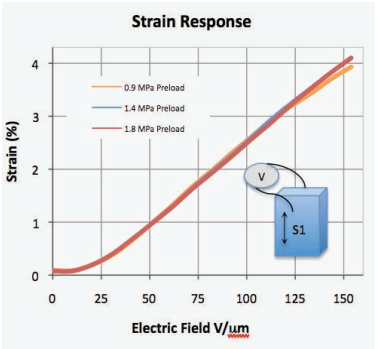


Figure B.6: Ferroelectric (a) and paraelectric (b) molecular configuration for P(VDF-TrFE-CFE) taken from [13]. -CFE is not shown in the plot. At room temperature, the alternating trans-gauche configuration that is non-polar is dominant. Under an electrical field, the polar molecules align with the field within one polymer segment and form the all trans conformation in (a). The black rods represent the carbon back bone and green segments are fluorine and the white segments are hydrogen.



SPS A3 EAP Film Properties	
Strain	2.5% (100V/micron)
Young's Modulus	700 MPa
Dielectric Constant	50 (20C and 1 KHz)
Dielectric Loss	5% (20C and 1 KHz)
Operating Temperature	0-50C
Thickness	3-10 microns

Figure B.7: The strain and electrical field relation and physical properties for a commercial available P(VDF-TrFE-CFE) terpolymer film SPS A3 from Strategic Polymers.

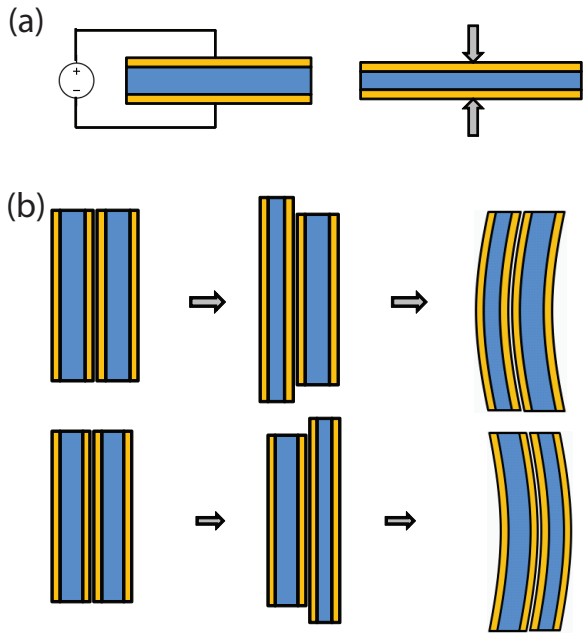


Figure B.8: (a) A unimorph structure under electrical field. The material can only extend in the direction of perpendicular to electrical field. (b) A bimorph structure whose bending directions can be controlled by applying field selectively on one side.

fect). Normally field is applied across the film thickness and the film contracts in the field direction and extends in the perpendicular direction (Fig. B.8 (a)). Prestretching the polymer along the film surface direction enlarges the strain in this direction due to alignment of molecules in this direction.[13] A bimorph structure is necessary to reliably control the bending directions (Fig. B.8 (b)).

The goal of this project is to create a 2D active-matrix thin film robot that can walk/swim to multi-directions. A directly addressed 3-segment 1D structure has been realized as the writing of this thesis. It uses bimorph structure for each segment and each segment is addressed through four high voltage Photo MOS relays (e.g., Panasonic AWV259). The unimorph on each side has two contacts for HIGH (charging) and LOW (discharging). All the connections are connected to and programmed in Arduino. A schematic plot of the electrical connections is shown in Fig. B.9. Fig. B.10 is the finished device with each segment bended independently.

The design of active matrix thin film actuator array is shown in Fig.B.11. Each element

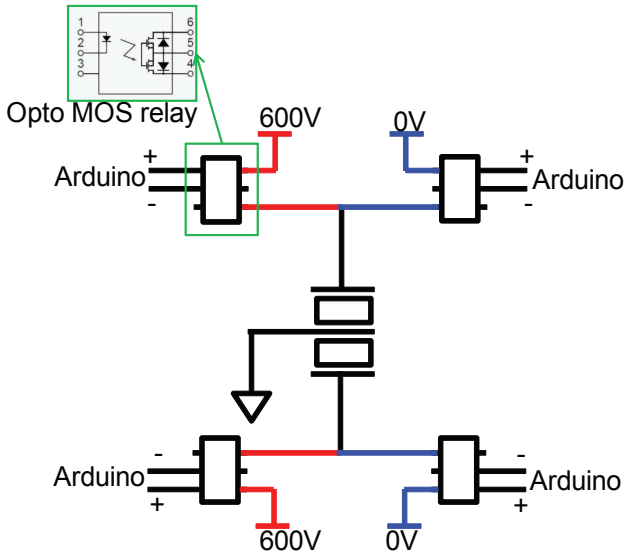


Figure B.9: A directly addressed 3-segment 1D structure has been realized. It uses bimorph structure for each segment which is addressed through four high voltage Photo MOS relays (e.g., Panasonic AWV259). The unimorph on each side of the bimorph has two contacts for HIGH (charging) and LOW (discharging). All the connections are connected to and programmed in Arduino.

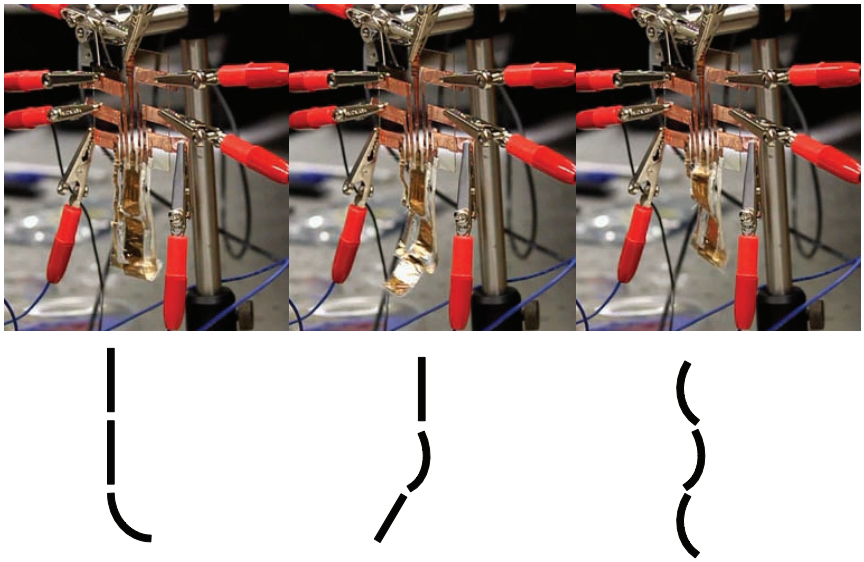


Figure B.10: Three segmented, directly addressed 1D bimorph strucuture bending independently.

has two transistors which control each unimorph respectively and simultaneously. The two column data buses can be combined into one. Active matrix operates in the following scheme: for each frame, row selector first turns on row 1, the column(s) apply voltage to the whole row simultaneously; then the row selector turns off row 1 and turn on row 2, and so on. To make clear the definitions of several terms, "charging" means to apply a high voltage across the terpolymer capacitor; "discharging" means to short both contacts across the terpolymer capacitor to ground; "leaking" means when the transistor is off, the charged terpolymer capacitor dissipates charges through the off resistance of the transistor and other paths. The frame refreshing rate needs to be slow enough for the capacitor to charge when its transistor is on and fast enough before the capacitor leaked away the charges when its transistor is off. Thus we have:

$$\frac{t_{frame}}{m_{row}} > \tau_{charging} \tag{B.2}$$

$$t_{frame} \cdot \frac{m_{row}-1}{m_{row}} < \tau_{leaking} \tag{B.3}$$

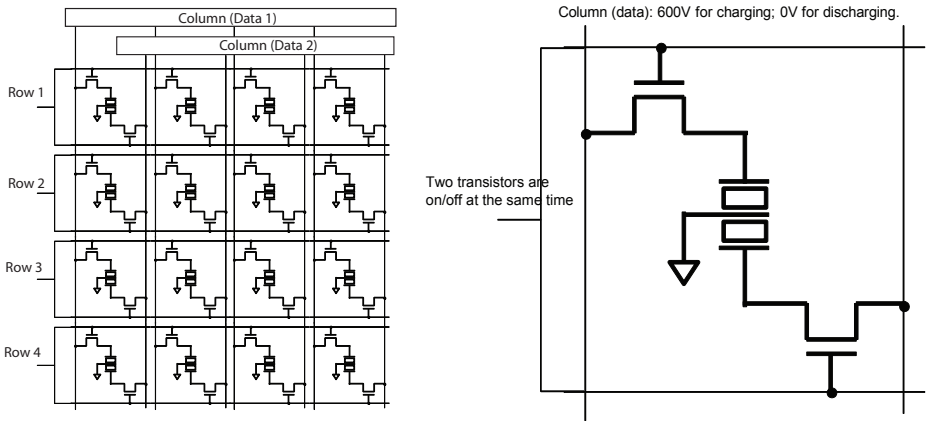


Figure B.11: The design of active matrix thin film actuator array and its single element.

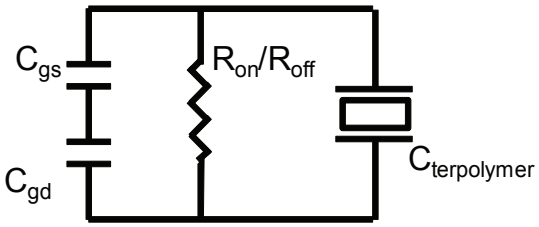


Figure B.12: RC component in the transistor-actuator integration.

where t_{frame} is the time per frame (e.g., for 10 frames per second, t_{frame} = 100 ms), m_{row} is the number of rows, $\tau_{charging}$ and $\tau_{leaking}$ are time constant for charging and leaking processes respectively.

Usually channel capacitance and overlap capacitance (source-gate, drain-gate) are much smaller than the terpolymer capacitance. For a 1 cm^2 × $1cm^2$ terpolymer capacitor, the capacitance is 4.4 nF, assuming the dielectric constant is 50 and the thickness is 10 μm. The channel capacitance and the overlap capacitance are all around several to several hundreds of pF. And the main RC component for charging and leaking process are the channel resistance and the terpolymer capacitance (Fig. B.12). Assuming $R_{on} = 10^6$ Ω and $R_{off} = 10^8$ Ω, $\tau_{charging}$ = 4.4 ms and $\tau_{leaking}$ = 440 ms. If there are 10 rows of devices, this means t_{frame} needs to be between 44 ms and 490 ms.